Performance Evaluation of Single and Three Phase 21-Level Symmetric Cascaded H-Bridge Multilevel Inverter using Level Shifted POD-PWM Technique

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Abstract - In this paper, the performance of simulated Single Phase and Three Phase 21-level Symmetric Cascaded H-bridge Multilevel Inverters was analyzed. In designing these inverters, a suitable level-shifted high-frequency pulse width modulation technique (POD PWM) was selected to meet the IEEE 519 total harmonic distortion requirement (of at most 5% for systems having bus voltage up to 69 kV), which is necessary for inverter deployment in renewable energy applications. The analysis was carried out using the high-frequency Phase Opposition Disposition (POD) level-shifted modulation technique, where a 50 Hz sinusoidal modulating signal was superimposed on a 1 kHz triangular carrier wave. Both signals had the same peak amplitude but different levels. The effect of variation in the modulation index (MI) on the percentage total harmonic distortion (%THD) was also carried out using the Discrete Fast Fourier Transform (DFFT) in MATLAB SIMULINK. The results show that the system's best performance occurred when it was modulated at 100%, as minimum THDs were obtained for single-phase (approximately 5.65%) and three-phase (approximately 3.68%) applications. Also, it was observed that the THD increased as the modulation index varied above and below its optimum value (100%). It was also validated that the Three-phase 21-level inverter has better THD (approximately 3.68% for A-phase, 3.55% for B-phase, and 3.64% for C-phase) compared to the single-phase 21-level inverter (having a THD of approximately 5.65%). This is due to the natural cancellation of triple odd-order harmonics, attributed to the symmetry involved in the inverter output voltage waveform, as reported in the literature.

Keywords: APOD, DFFT, H-Bridge , MI , Multi-Levels, PD, POD, PS, PWM, SHEPWM , Single Phase, THD , Three- Phase

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I. Introduction

A multilevel inverter synthesizes a sinusoidal voltage using different levels [1]-[2]. Multilevel inverters are broadly classified into three types based on switch configurations [3]: Diode-clamped (sometimes called neutral point clamped or NPC), Cascaded H-bridge (CHB), and Flying Capacitor (FC) multilevel inverters. A three-phase inverter is a modification of the single-phase inverter, consisting of three identically connected single-phase unit of the inverter, each generating an output voltage that is 120 degrees out of phase from another. Phase-shifted and level-shifted PWM are the most commonly used control techniques for multilevel inverters [4]. The POD modulation scheme, which is a level-shifted PWM technique, is adopted in this work as it yields a better percentage THD compared to other high-frequency modulation techniques [5]. Multilevel inverters are aimed at reducing the total harmonic distortion (THD) of the output voltage.

A 33-level asymmetrical cascaded H-bridge multilevel inverter using high-frequency PWM techniques was presented for medium power applications, employing different modulation techniques. According to [3], the phase disposition pulse width modulation (PDPWM) yields a better THD for 100% modulation, whereas the variable frequency carrier (VFCPWM) yields lesser THD at 40% modulation. The authors in [1] presented a 7-level symmetrical multilevel inverter for photovoltaic applications using both PWM and high-frequency modulation techniques so as to reduce the number of switching states and the THD of the output voltage. [6] carried out low-frequency modulation using selective harmonics elimination PWM (SHEPWM) for a three-level flying capacitors inverter, which systematically eliminated the higher-order harmonics while maximizing the fundamental output voltage. The authors in [7] presented a new topology for a three-phase nine-level inverter as a Capacitor Clamped H-Bridge (CCHB) three-phase Multilevel Inverter (MI) that was designed to generate a nine-level three-phase AC output voltage according to suitable control (gate) signals. [8] proposed a modified three-phase inverter from the developed H-bridge structure having multilevel functionality. The topology can generate 7-levels of phase voltages and 13-levels of line voltages [9] suggested a new topology for a three-phase multilevel inverter (MLI) with Common Mode Voltage (CMV) elimination

II. The 21-Level Three-Phase Symmetric CHB Inverter Topology

The symmetrical Three-Phase CHB Inverter proposed in this work can generate 21 voltage levels at its output using bidirectional switches when controlled appropriately [10]-[11]. For a symmetric CHB inverter to generate 21 output levels, ten independent DC sources are required. Although the number of these independently connected DC sources can be reduced by using asymmetrical structures, the THD and the voltage stress on each switching device will increase as a consequence [12]. Also, there is unequal power sharing between each bridge in the asymmetric structure, which requires a power equalization circuit to maintain power balance [13]-[14]. The proposed 21-level symmetric CHB inverter structure, showing one phase of the inverter, is presented in Fig. 1, while the complete block representation of the Three-Phase 21-Level Cascaded H-bridge Inverter is depicted in Fig. 2. The Fourier series decomposition of the inverter output voltage waveform in Fig. 3, according to [10], is given in (1).

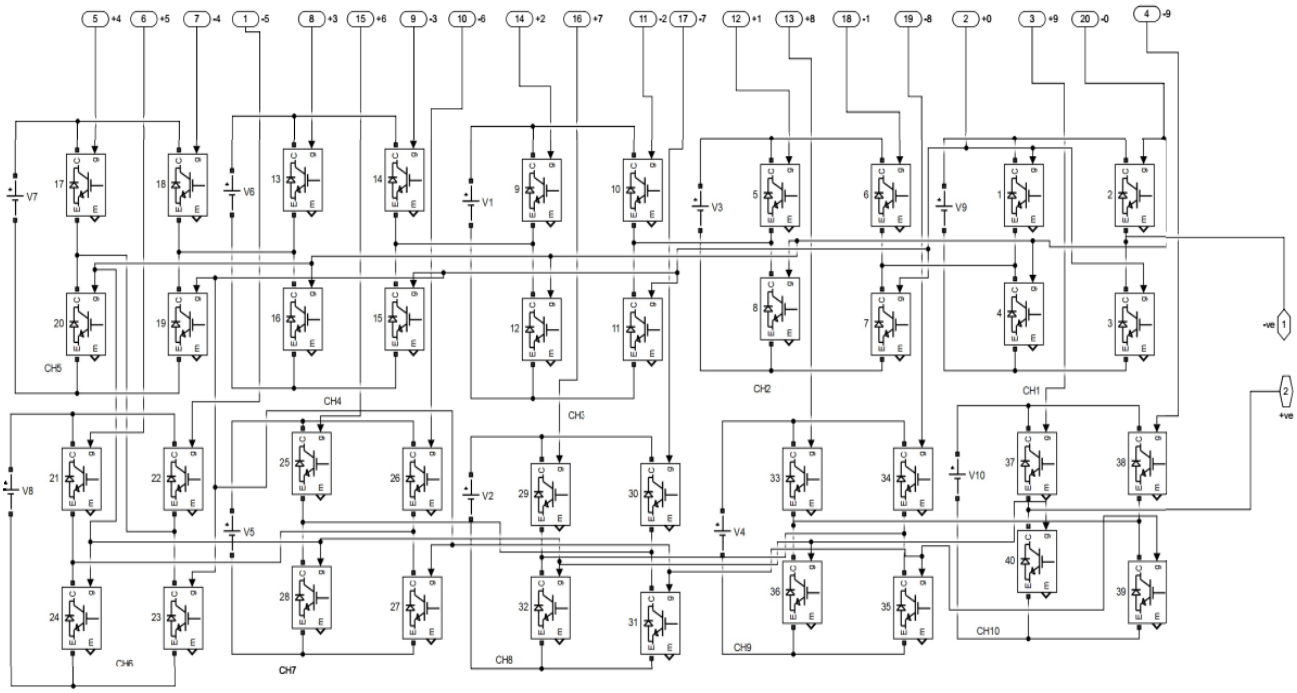

Fig. 1. The Single-Phase Structure of the 21-Level Inverter

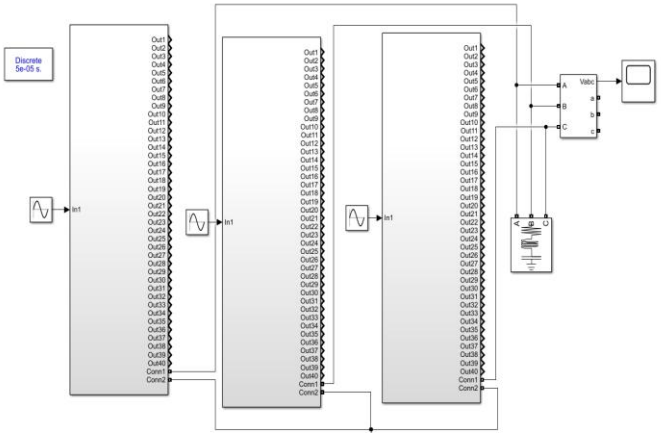

Fig. 2. Three-Phase Structure of the 21-Level Inverter

With reference to Fig.1, there are ten cascaded H-bridges in series each having a dc bus voltage link of V and each generating an output voltage of $-V_{dc}$, 0, and $+V_{dc}$. The algebraic sum of these voltages is the output voltage of the inverter having the voltage levels:

$-10V_{dc}$, $-9V_{dc}$, $-8V_{dc}$, $-7V_{dc}$, $-6V_{dc}$, $-5V_{dc}$, $-4V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, 0, V_{dc}, $2V_{dc}$, $3V_{dc}$, $4V_{dc}$, $5V_{dc}$, $6V_{dc}$, $7V_{dc}$, $8V_{dc}$, $9V_{dc}$, and $10V_{dc}$. The output voltage waveform of the inverter is said to have quarter-wave odd symmetry [15]. The switching table of the inverter is given in Table 1. It is important to note that the proposed three-phase inverter structure is obtained by connecting the single-phase structure in a star configuration to supply a three-phase load.

$$V_{21} = \frac{4V_{dc}}{\pi}\sum_{n=1}^{\infty}(\cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \ldots \cos\theta_{10})\frac{\sin(n\omega t)}{n} \quad (1)$$

Where:V_{21} is the complex generated by the 21-level inverter, $\theta_1, \theta_2, \theta_3 \ldots \theta_{10}$ are the respective phase delays, n is the harmonic number, ω is the angular frequency, and V_{dc} is external DC voltage

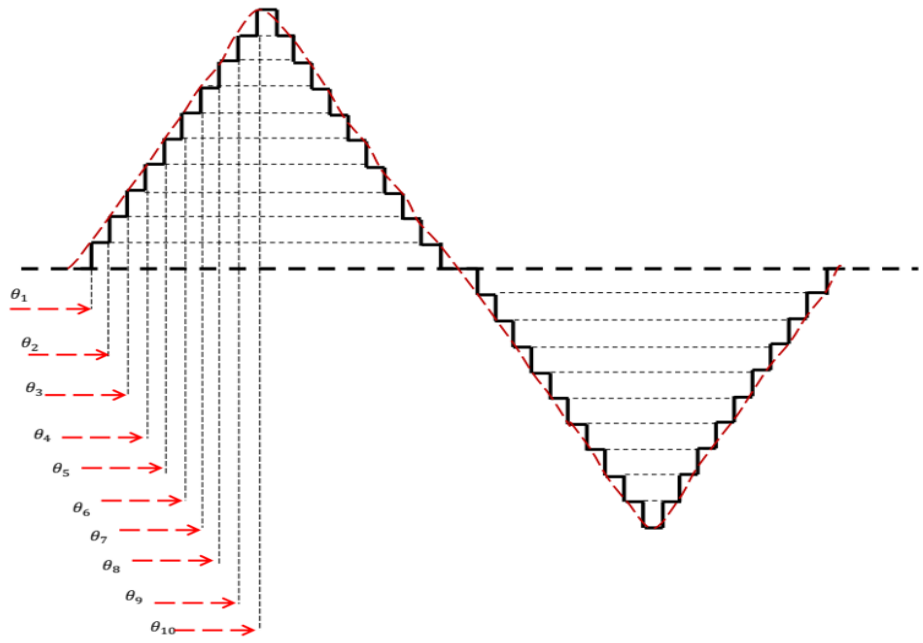

Fig. 3. The Inverter Voltage Waveform

III. Integration of DC-DC Boost Converter

The inverter DC energy is supplied from a battery whose output voltage (typically 12V or 24V) is not sufficient to generate a desired output of 1.6kV. Hence, there is a need to incorporate a boost converter [16]-[17].

producing an output voltage greater than its input voltage [17]-[18]. A closed-loop controlled 12V/200V DC-DC boost converter, shown in Fig. 4, is used as the source of DC energy supply that is powered from photovoltaic (PV) source for each H-bridge cell of the 21-level symmetric cascaded H-bridge multilevel. inverter.

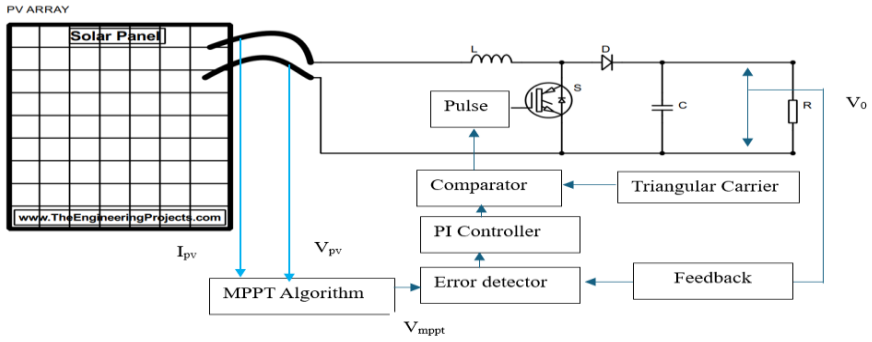

Fig. 4. The Close Loop Control DC-DC Boost Converter

TABLE 1

SWITCHING TABLE OF THE 21-LEVEL INVERTER

Active Switches	Incoming Switch	Outgoing Switches	Voltage Level
3,7,11,13,15,19,23,27,31,35,39	-	2,4,8,12,16,20,24,28,32,36,40, 6,10,14,18,22,26,30,34,38	0
3,7,11,13,15,19,23,27,31,35,39	1	-	+V
3,7,11,13,15,19,23,27,31,35,39,1	5	-	+2V
3,7,11,13,15,19,23,27,31,35,39,1,5	9	-	+3V
3,7,11,13,15,19,23,27,31,35,39,1,5,9	13	-	+4V
3,7,11,13,15,19,23,27,31,35,39,1,5,9,13	17	-	+5V
3,7,11,13,15,19,23,27,31,35,39,1,5,9,13,17	21	-	+6V
3,7,11,13,15,19,23,27,31,35,39,1,5,9,13,17,21	25	-	+7V
3,7,11,13,15,19,23,27,31,35,39,1,5,9,13,17,21,25	29	-	+8V
3,7,11,13,15,19,23,27,31,35,39,1,5,9,13,17,21,25, 29	33	-	+9v
3,7,11,13,15,19,23,27,31,35,39,1,5,9,13,17,21,25, 29,33	37	-	+10V
2,4,8,12,16,20,24,28,32,36,40	-	3,7,11,13,15,19,23,27,31,35,39 ,1,5,9,13,17,21,25,29,33,37	-V
2,4,8,12,16,20,24,28,32,36,40	6	-	-2V
2,4,8,12,16,20,24,28,32,36,40,6	10	-	-3V
2,4,8,12,16,20,24,28,32,36,40,6,10	14	-	-4V
2,4,8,12,16,20,24,28,32,36,40,6,10,14	18	-	-5V
2,4,8,12,16,20,24,28,32,36,40,6,10,14,18	22	-	-6V
2,4,8,12,16,20,24,28,32,36,40,6,10,14,18,22	26	-	-7V
2,4,8,12,16,20,24,28,32,36,40,6,10,14,18,22,26	30	-	-8V
2,4,8,12,16,20,24,28,32,36,40,6,10,14,18,22,26,3 0	34	-	-9V
2,4,8,12,16,20,24,28,32,36,40,6,10,14,18,22,26,3 0,34	38	-	-10V

IV. Inverter Control Strategies

Generating the 21-level requires a special control mechanism to appropriately apply the gate pulse to the switching devices [19]-[20]. The modulation technique used is level-shifted PWM. To analyze the performance of the three-phase 21-level asymmetric CHB inverters using the aforementioned control technique, a 50Hz sinusoidal modulating signal is superimposed on 10 triangular carrier signals, each operating at 1kHz. This was implemented in MATLAB using Simulink block models, as shown in Fig. 5. The signal generated during this time by applying the POD PWM control is shown in Fig. 6.

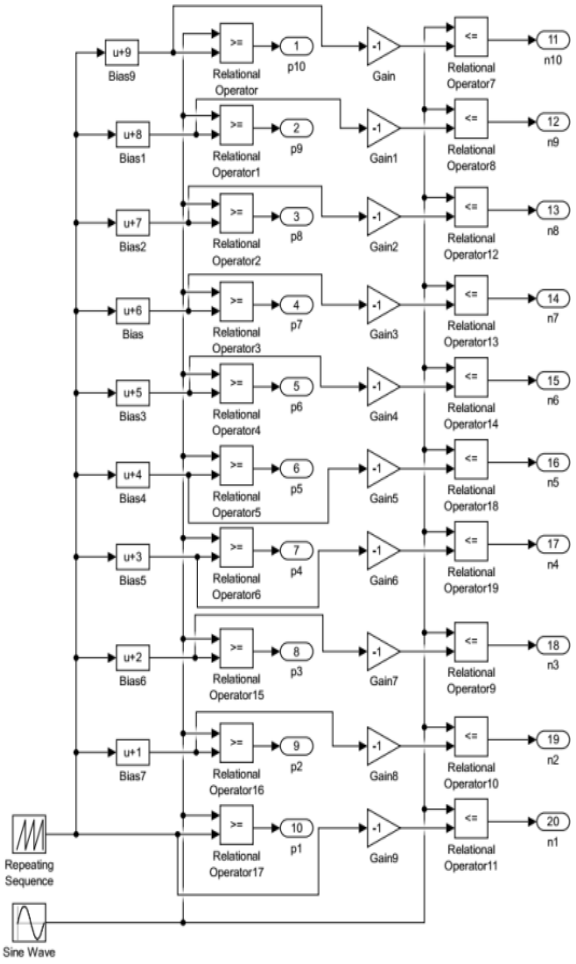

Fig. 5. The PWM Modulator

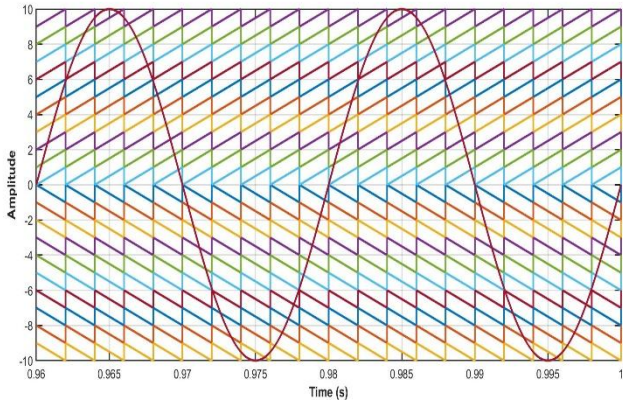

Fig.6. The Generated Level Shifted POD PWM Signals

Note that in the implementation of high-frequency POD PWM, the carrier signals, which are set at 1kHz, are level-shifted and compared with a sinusoidal modulating signal, which is set at the desired fundamental frequency of 50 Hz. The amplitude of the triangular carrier signals is set at 1V each, while the modulating signal amplitude is set to 10V, appropriate for the generation of the control signal of the 21-level inverter [21]-[22].

V. Simulations and Results

The simulation results for the 21-level inverter structure, powered by a 200V DC-DC Boost Converter and simulated at 100% modulation using POD PWM control, are presented in Figures 7-10 for both single-phase and three-phase operations.

Figure 7 illustrates the output voltage generate
d by the single-phase inverter, which displays a staircase waveform with 21 levels. Figure 8 presents the Fast Fourier Transform (FFT) decomposition of this single-phase inverter output, revealing a Total Harmonic Distortion (THD) of 5.65%.

For the three-phase configuration, Figure 9 shows the generated three-phase signal when the single-phase inverter is connected in a three-phase arrangement. Figure 10 provides the FFT analysis of this three-phase signal, indicating that the three-phase inverter achieved a superior THD of approximately 3.68%, which is notably better than the single-phase equivalent.

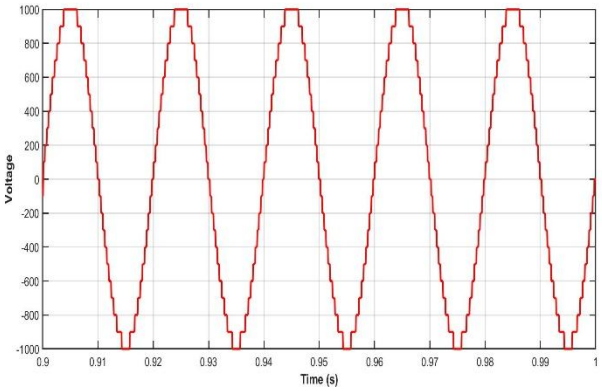

Fig. 7. The Single Phase Inverter Output Voltage

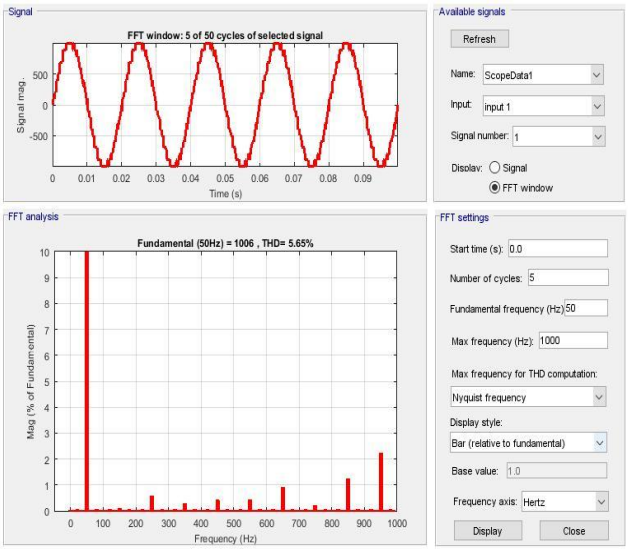

Fig. 8. The DFFT Analysis of Single-Phase Inverter Output

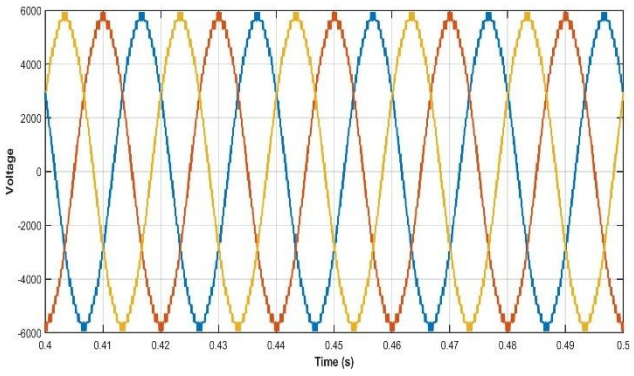

Fig. 9. The Three Phase Inverter Output Voltage

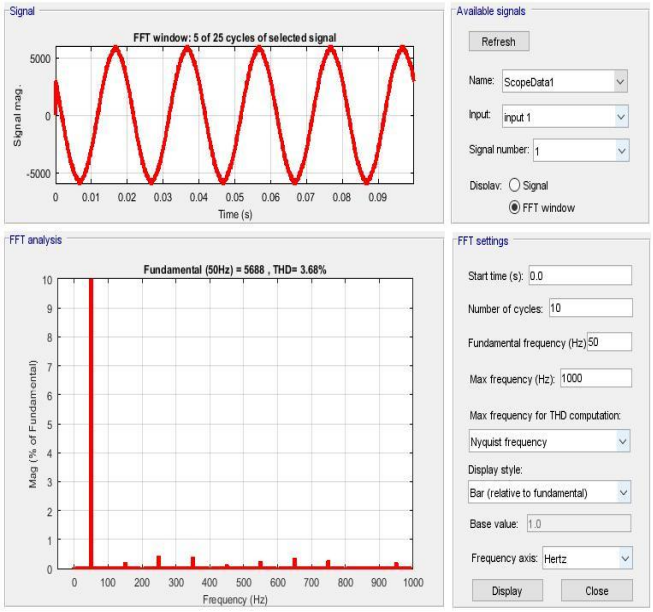

Fig. 10. The DFFT Analysis of Three Phase Inverter Output

VI. Effect of Modulation Index on THD

When the amplitude of the modulating signal is **v**aried, the modulation index, which is the ratio of the peak amplitude of the modulating signal to the sum of the peak amplitudes of the triangular carriers, changes proportionately. Table 2 shows the variation of the THD per phase of the inverter by varying the modulation index, and it can be seen that the modulation index has a profound effect on the THD, as shown in Fig. 11.

TABLE 2

EFFECT OF MODULATION INDEX ON THD

Modulation Index (%)	THD Single-Phase	THD Three-Phase		
		A	B	C
120%	8.67%	5.02%	5.60%	5.00%
100%	5.65%	3.68%	3.55%	3.64%
80%	6.53%	4.75%	5.39%	4.72%
60%	9.29%	6.15%	6.55%	6.15%
40%	13.72%	8.89%	8.93%	8.89%
20%	26.03%	18.62%	19.01 %	18.61%

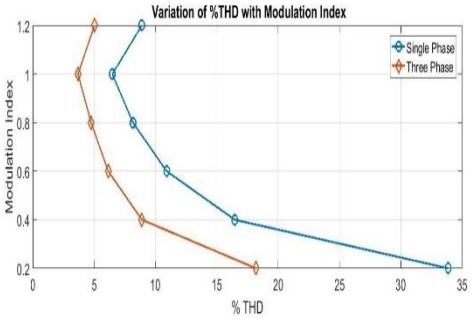

Fig. 11. Variation of % THD with % MI

VII. Discussion of Results

From the THD plot in Fig. 10, it's clear that the three-phase 21-level inverter consistently exhibits superior THD performance across all variations of the modulation index (between 0.2 and 1.2) when compared to the single-phase 21-level inverter. This improvement is attributed to the inherent cancellation of triple harmonics when the inverter operates in a three-phase configuration, which significantly reduces the overall THD.

Furthermore, a notable improvement in THD was observed for single-phase applications in this work. A minimum THD of 5.65% was obtained, which is better than the 6.13% reported in [11] using the same modulation technique. This indicates a significant enhancement in performance in the current study.

VIII. Conclusion

This paper has successfully investigated the performance of a Single-Phase and Three-Phase 21-level symmetric CHB inverter using the POD PWM technique. Based on FFT analysis, minimum THDs for both Single-Phase and Three-Phase were obtained at 100% modulation. These harmonics increased as the modulation index was varied around its optimum. The Three-Phase inverter has better THD than the Single-Phase inverter due to harmonic cancellation resulting from the phase shift between the modulating signals and the way the harmonics are distributed across the line-line voltage. The analysis was successfully carried out in MATLAB and the SIMULINK environment. Also when compared with the work of [11], THD of 5.65% was obtained, as against its 6.13% for same modulation index which shows a significant improvement in this work.

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Conflict of Interest

The authors declare no conflict of interest in the publication process of the research article.

Author Contributions

M.J. Deshi carried out the design and the implementation of the inverter in MATLAB SIMULINK. He also writes the manuscript

E.C., Anene, J.T. Agee and S.M. Hassan supervised the work and they provided their professional knowledge in writing the manuscript

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