Impedance network based isolated three-phase AC-AC converter with enhanced voltage gain and safety

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Abstract – The conventional matrix converter has limited voltage gain and requires a large number of switches. The Ultra Sparse Matrix Converter (USMC) was introduced to address this, reducing the number of switches. However, its voltage gain remains significantly low, and being non-isolated, it also raises safety concerns. This paper focused on achieving higher voltage gain, providing electrical isolation, and reducing the switching voltage stress. In this paper, a novel three-phase isolated duodecuple source (DS) impedance network-based USMC is proposed. The DS impedance network consists of a flyback stage with high-frequency transformer isolation, a boost stage, and a voltage tripler stage. The flyback stage provides electrical isolation, the boost stage enhances voltage gain, and the voltage tripler stage makes it triple. Simulation results show that with an input of 220 V AC, the proposed DS-USMC delivers an isolated three-phase output of 2640 V AC, achieving a voltage gain of 12 at a duty ratio of 0.5, compared to the conventional USMC gain of 0.867. The inductor current remains stable with a peak of 12 A, and the maximum voltage stress across the DS switches is 30V and 61V, well below the critical threshold. The proposed DS-USMC retains all the merits of their existing USMC, providing a larger range of output voltage with electrical isolation, safety, and reducing switching voltage stress in a cost-effective manner.

Keywords*: High Frequency Transformer (HFT), Isolated AC-AC converter, Isolated Power Converter, Three Phase AC-AC converter, Ultra Sparse Matrix Converter (USMC), Voltage Gain Enhancement.*

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I. Introduction

The AC-AC converter can be classified into three main types: direct pulse width modulation AC-AC converters [1], indirect AC-AC converters with a DC link [2], and matrix converters [3] – [4]. The indirect AC-AC converter with a DC link is an upgraded version of the matrix converter [5]. It reduces the number of switches and incorporates a DC link, which is known as an impedance network. This converter is referred to as the Ultra Sparse Matrix Converter (USMC) [6] – [7]. USMC is more popular among all AC-AC converters for its capability of generating variable output voltage and frequency [8]. However, the voltage gain of USMC is not ideal, approximately 0.867 [9]. This lower voltage gain acts as a barrier to make this converter suitable for universal usage in industries and renewable energy integration into the grid [10]. To overcome this difficulty, researchers have proposed various USMCs, including ZS-USMC, SZS-USMC, QZ-USMC, DB-USMC, SIZ-USMC, and SB-USMC [11] – [14]. These converters are significantly upgraded over the typical USMC in terms of voltage gain, passive elements, and voltage stress across switches. However, these existing USMCs are not isolated. Non-isolated USMCs have serious safety issues, especially in industrial and renewable energy applications, as there is a direct connection between the rectifier and inverter stages [15]. To provide electrical isolation for safety, external bulky line-frequency transformers are required [16]. These line transformers have several drawbacks, such as being bulkier, high cost, saturation issues, and high inrush current. They also increase load voltage harmonics, which become more dangerous for non-linear loads [17].

To overcome these limitations, a high-frequency transformer-isolated (HFTI) Z-Source AC-AC converter was proposed in [18]. However, it is single-phase, and an additional single-phase-to-three-phase converter is required for grid integration [19]. Additionally, it has limited voltage gain [20]. To overcome these limitations, researchers proposed modified three-phase HFTI converters, which have some major limitations, including insignificant voltage gain, higher output voltage ripple, and higher voltage stress across switches [21] – [22]. To address these drawbacks, researchers proposed various isolated DC link USMCs. All existing isolated USMC converters have their relative merits and demerits, but the most notable limitation of all USMC converters is that the voltage gain is significantly lower and the voltage stress across switches is much higher [23] – [24]. Therefore, we need higher voltage gain and lower voltage stress to meet the requirements of modern power systems and renewable energy systems. However, achieving the higher voltage gain with lower voltage stress across switches remains a significant challenge.

To address this challenge, we proposed an isolated duodecuple source (DS) Ultra Sparse Matrix Converter (DS-USMC) by integrating a novel isolated duodecuple source impedance network into the USMC. The proposed DS-USMC uses the DS concept that originates from the boost circuit, voltage tripler, and flyback converter. The DS impedance network has three stages: the flyback stage, boost, and the voltage tripler stage. Additionally, to further reduce the voltage stress across switches, the external RCD snubber circuit in parallel with the switches is used. We simulated the proposed DS-USMC using MATLAB Simulink 2020a software. Finally, the simulation results show that the proposed DS-USMC converter has a voltage gain of 12 at a 50% duty ratio. The voltage stress was reduced significantly and remained below the threshold point.

We organized the paper as follows: 1) Section II describes the proposed DS-USMC topology with a detailed description of the duodecuple source network and the formulation of the mathematical background. 2) Section III explains the switching strategy of the proposed topology. 3) Section IV includes the design considerations of the proposed DS-USMC topology. 4) Sections V and VI cover the methodology, testing and validation, simulation results, and a summary of the parameter values used. 5) Section VII compares the proposed topology with the other types of USMC. 6) Section VIII concludes the paper with future directions.

II. Proposed Topology

The proposed DS-USMC is shown in Fig. 1. It consists of three stages: a rectifier stage on the left, an impedance network at the center, and an inverter stage on the right. The Duodecuple Source (DS) converter is used as the impedance network. The rectifier stage comprises three unidirectional switches (Sa, Sb, and Sc) and 12 power diodes connected to the three-phase supply at points a, b, and c. Inductors and capacitors, connected to each phase, act as filters to reduce harmonic distortion. This stage is capable of converting the three-phase AC voltage into DC while enhancing the voltage gain by a factor of 1.5 [8]. The output section of the rectifier stage, denoted as V_{rtf}, is connected to the DS impedance network. Details about the DS converter are provided in subsection A. The DS converter enhances the rectified DC voltage by a factor of 12.

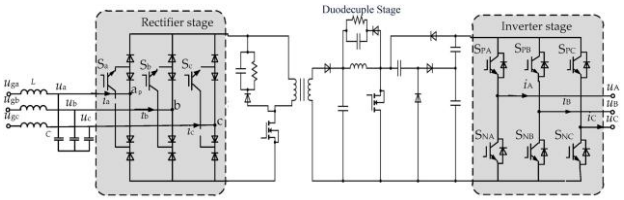

Fig. 1. The Proposed DS-USMC Converter Topology

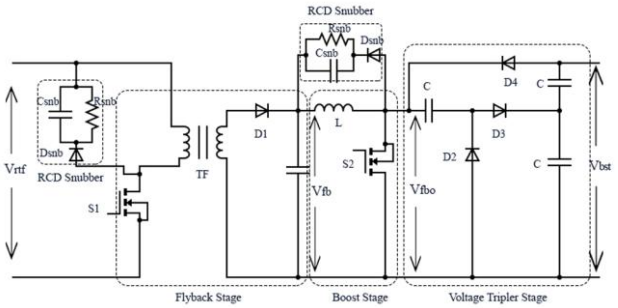

Fig. 2. Duodecuple Source (DS) Impedance Network

The output section of the DS converter is directly connected to the inverter stage. The inverter stage comprises six switches, denoted as S_{PA}, S_{NA}, S_{PB}, S_{NB}, S_{PC}, and S_{NC}. This stage converts the boosted DC voltage back into AC while reducing the voltage gain by a factor of 0.57 [8]. The output voltages are represented as V_A, V_B, and V_C. The performance of the proposed DS-USMC is evaluated using MATLAB Simulink software. The operation of the DS converter, the optimized switching strategy, and the design consideration of passive elements are detailed in the following sections.

A. Duodecouple Source Impedance Network

The Duodecuple Source (DS) converter is the impedance network of the proposed DS-USMC converter topology, which is a step-up isolated converter with dynamic behavior similar to that of an isolated boost converter. As shown in Fig. 2, the DS converter comprises three substages: the flyback stage, the boost stage, and the voltage tripler stage.

In the flyback stage, a high-frequency (HF) transformer is used to provide the electrical isolation between the input and output sections. The input voltage of the DS converter is denoted as V_{rtf} . The output voltages of the flyback, boost, and voltage tripler stages are denoted as V_{fb}, V_{fbo}, and V_{bst}, respectively. The HF transformer has a turn ratio of 1:2. To reduce the voltage stress across switches S_1 and S_2, two RCD snubbers are used externally.

The operation of the DS converter is described in two modes: shoot-through (ST) mode and non-shoot-through (NST) mode. The ST mode begins when switch S_2 is turned ON. During this mode, diodes D_2, D_3, and D_4 are OFF, and the inductor L stores energy. When S_2 is turned OFF, the system transitions to the NST mode, during which diodes D_2, D_3, and D_4 are ON, and the inductor releases the stored energy. Switch S_1 controls the power supply to the HF transformer.

The voltage across the inductor is

$$V_L = L\frac{di_L}{dt} \tag{1.1}$$

$$di_L = \frac{V_L}{L}dt \tag{1.2}$$

For flyback stage, when switch S_1 = ON,

$$\Delta i_{on} = \frac{V_{ref}}{L}D_S T \tag{1.3}$$

When switch S_1 = OFF

$$\Delta i_{off} = -\frac{V_{fb}}{nL}\left(1-D_S\right)T \tag{1.4}$$

where

n= transformer turn ratio = $n_{secondary}/n_{primary}$

D_s = duty ratio

As the current of the complete cycle is zero,

$$\Delta i_{on} + \Delta i_{off} = 0 \tag{1.5}$$

$$\frac{V_{ref}}{L}D_S T - \frac{V_{fb}}{nL}\left(1-D_S\right)T = 0 \tag{1.6}$$

$$V_{ref}D_S = \frac{V_{fb}}{n}\left(1-D_S\right) \tag{1.7}$$

$$V_{fb} = \frac{V_{ref}}{1-D_S}\times n \tag{1.8}$$

Here, V_{fb} is the output voltage of the flyback stage. This voltage will act as the input voltage for the boost stage.

For boost stage, when switch S_2 is ON, then diodes D_2, D_3, and D_4 are off and vice versa. So, the boost stage & voltage tripler stage cannot be ON at the same time. Applying KVL to the boost stage when S_2 = ON

$$V_{fb} - V_L = 0 \tag{1.9}$$

For, S_2 = OFF

$$V_{fb} - V_L - V_{fbo} = 0 \tag{1.10}$$

V_{fbo} is the output voltage of the boost stage, which will feed the voltage tripler circuit.

As a voltage tripler circuit enhances the output voltage three times in input voltage, so

$$V_{bst} = 3V_{fbo} \tag{1.11}$$

$$V_{fb} - V_L - \frac{V_{bst}}{3} = 0 \tag{1.12}$$

Now

$$\int_0^T V_L dt = 0 \tag{1.13}$$

$$V_{bst} = \frac{3V_{ref}}{\left(1-D_S\right)^2}\times n \tag{1.14}$$

Here, the overall output voltage duodecuple source converter is V_{bst}.

Now, the maximum phase output voltage of the inverter stage is

$$V_{ABC} = \frac{M_S}{\sqrt{3}}V_{bst} \tag{1.15}$$

where M_s is the modulation index.

Considering the power factor, the overall voltage gain of the proposed DS-USMC is

$$\frac{V_{ABC}}{V_{abc}} = \frac{\sqrt{3}M_S \times 3V_{ref}\ D_S}{\left(1-D_S\right)^2} \times n\cos\tau \qquad (1.16)$$

$$\frac{V_{ABC}}{V_{abc}} = \frac{3\sqrt{3}}{2} \times \frac{M_S D_S}{\left(1-D_S\right)^2} \times n\cos\tau \qquad (1.17)$$

where τ is the angle between voltage and current.

The boosting factor is

$$B_f = \frac{3\sqrt{3}}{2} \times \frac{D_S}{\left(1-D_S\right)^2} \times n \qquad (1.18)$$

$$D_S = \frac{2B_f(1-D_{S)}{}^2}{3\sqrt{3}\,D_s n} \qquad (1.19)$$

III. Switching Strategy

The optimization of three-phase power converter efficiency and performance depends on the switching strategy employed in the rectifier and inverter stages. Here, we have used State Vector Pulse Width Modulation (SVPWM) to generate control signals for the rectifier and inverter stages of the proposed DS-USMC topology. In this switching strategy, a PWM signal has to be attached to the state vector diagram. This diagram is shown in Fig. 3. In the rectifier stage, there are six active vectors: I_{pq}, I_{qr}, I_{rp}, I_{qp}, I_{rq}, I_{pr}, and three zero vectors: I_{pp}, I_{qq}, I_{rr}. For the inverter stage, there are six active vectors: V_{001}, V_{010}, V_{011}, V_{100}, V_{101}, V_{110}, and two zero vectors: V_{000} and V_{111}. To apply SVPWM in both the rectifier and inverter stages, I_{ref} can be adjusted by two active vectors, and V_{ref} by a combination of active and zero vectors. Duty ratio for both stages vectors are shown in equations (1.20) – (1.23).

$$DI_{pq} = \frac{\sin\left(\frac{\varphi}{3} - l\right)}{\cos i} \qquad (1.20)$$

$$DV_{001} = \sin\left(\frac{\varphi}{3} - \psi\right) \qquad (1.21)$$

$$DI_{pr} = \frac{\sin(l)}{\cos i} \qquad (1.22)$$

$$DV_{010} = \sin(\psi) \qquad (1.23)$$

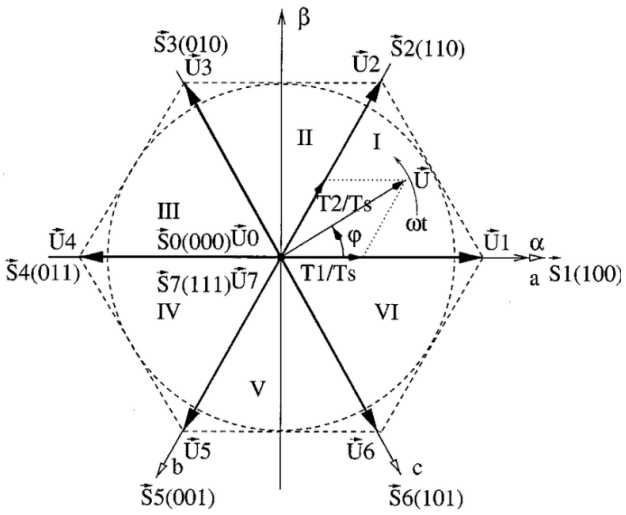

Fig. 3: Space Vector diagram for SVPWM switching technique [26]

Here ℓ and ψ is the sector angle of the rectifier stage and vector angle of the inverter stage. We can define other active vectors such as D_{iqr} and DV_{011} in the same way. The overall duty ratio of the DS-USMC is presented in the following equation.

$$D_w = DI_{pq} * DV_{001} \qquad (1.24)$$

$$D_x = DI_{pq} * DV_{010} \qquad (1.25)$$

$$D_y = DI_{pr} * DV_{010} \qquad (1.26)$$

$$D_z = DI_{pr} * DV_{001} \qquad (1.27)$$

$$D_m = 1 - D_w - D_x - D_y - D_z \qquad (1.28)$$

The switching pattern of the DS-USMC is shown in Table I.

TABLE I
SWITCHING STRATEGY OF DS-USMC

Non Shoot Through			*Shoot Through*		
I_{pq}	V_{000}	D_m /4	I_{pr}	V_{000}	D_m /4
	V_{001}	D_w /2		V_{001}	D_z /2
	V_{010}	D_x /2		V_{010}	D_y /2
I_{pr}	V_{010}	D_y /2	I_{pq}	V_{010}	D_x /4
	V_{001}	D_z /4		V_{001}	D_w /2
	V_{000}	D_m /2		V_{000}	D_m /2

IV. Passive Elements Selection

The passive elements of the topology are calculated based on the ripple current across the inductor and ripple voltage across the capacitor, using the boundary condition of continuous conduction mode (CCM) [27], as in equation (1.29)

$$V_L = L\frac{di_L}{dt} = L\frac{\Delta i_L}{\Delta t} \tag{1.29}$$

$$\Delta t = DT \tag{1.30}$$

where

$$T = \frac{1}{f} \tag{1.31}$$

$$\Delta i_L = \frac{D_S T V_{ref}}{L} \tag{1.32}$$

According to the CCM

$$I_L - \frac{1}{2}\Delta I_L = 0 \tag{1.33}$$

$$I_L = \frac{D_S T V_{ref}}{2L} \tag{1.34}$$

Now

$$p_{out} = V_{bst} I_L \tag{1.35}$$

$$L = \frac{D(1-D)V_{bst}^{\ 2}}{6 f P_{out} n} \tag{1.36}$$

Considering % the ripple and power factor

$$L = \frac{D(1-D)V_{bst}^{\ 2}\cos\tau}{6 f \ \%a P_{out} n} \tag{1.37}$$

On the other side

$$I_C = C\frac{\Delta V_C}{\Delta t} \tag{1.38}$$

$$C = \frac{\Delta t\, I_C}{\Delta V_{ref}} \tag{1.39}$$

$$C = \frac{D_S T I_C}{V_{ref}^{\ 2}} \tag{1.40}$$

$$C = \frac{D_S T P_{out}}{V_{ref}^{\ 2}} \tag{1.41}$$

$$C = \frac{D_S T P_{out}}{V_{ref}^{\ 2}\ \%x \cos\tau} \tag{1.42}$$

This equation gives the required value of C for %x ripple & P_{out} power.

For the RCD snubber, all parameters are introduced in [28].

$$C_{snb} = \frac{2P_R}{V_{snb}^{\ 2} f_s} \tag{1.43}$$

$$R_{snb} = \frac{DT V_{snb}^{\ 2} f_s}{8P_R} \tag{1.44}$$

Here, C_{snb} and R_{snb} is the snubber capacitance & resistance.

V. Methodology

The Proposed DS-USMC is simulated and validated using MATLAB Simulink R2020a. Firstly, the DS-USMC is designed in MATLAB Simulink based on the circuit diagram, shown in Fig. 1. Thereafter, all parameter values are assigned, as listed in Table II. The values of inductor and capacitor were calculated as L= 0.5µH and C= 10µF, using the equations (1.37) and (1.42), respectively, with 1.5625% and 0.3185% ripple

factors. The duty ratio (D_s) and switching frequencies were selected as 0.5, 25 kHz, and 40kHz. Finally, the switching pattern is applied, with details provided in section III.

VI. Simulation Results

A 220V three-phase AC voltage is supplied as the input source to the proposed DS-USMC, as shown in Fig. 4. After passing this input voltage through the rectifier stage of the proposed converter, the output DC voltage at the rectified stage is 332V, as demonstrated in Fig. 5. This value slightly deviates from the theoretical value of 330V due to the use of inductors and capacitors in the input section as filters. The rectified voltage feeds the duodecuple source (DS) stage, where the output voltage is 3980V, as shown in Fig. 6. This is 12 times higher than the rectified stage voltage.

The peak current across the inductor is 12A, as illustrated in Fig. 8. The maximum voltage stress across switches S_1 and S_2 is 30V and 61V, respectively, as shown in Fig. 7. These voltage stress levels are safely below the critical threshold.

Finally, at the inverter stage, the output three-phase AC voltage is 2640V, as shown in Fig. 9. Overall, the final output three-phase AC voltage is 12 times higher than the input AC source voltage at a duty ratio of 0.5. By varying the modulation index or duty ratio, a variable voltage can be achieved, provided the condition of $M_s+D_s \leq 1$.

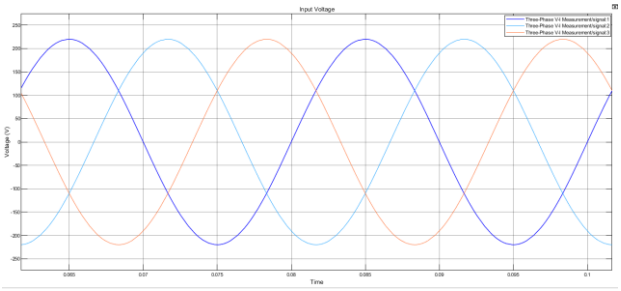

Fig. 4. Three Phase AC input voltage

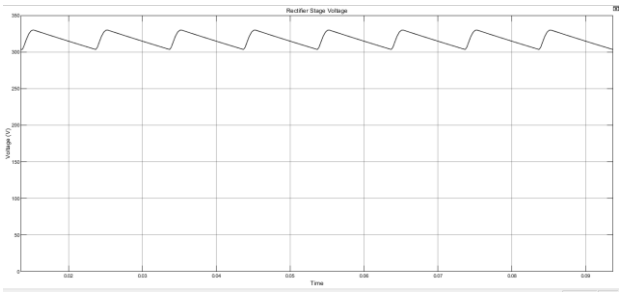

Fig. 5. Output Waveform of Rectifier Stage

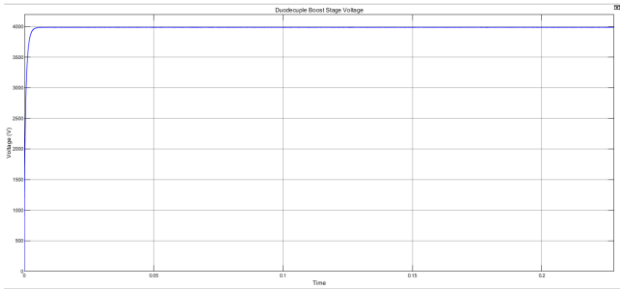

Fig. 6. Output Waveform of the Duodecuple Source Stage

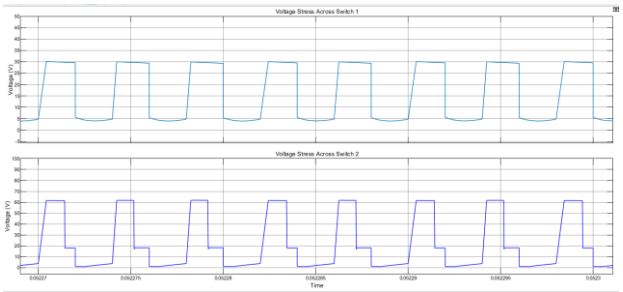

Fig. 7. Voltage Stress Across the Switches (S_1 and S_2)

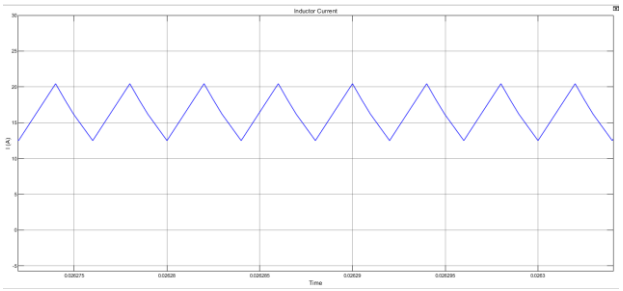

Fig. 8. Current Across Inductor

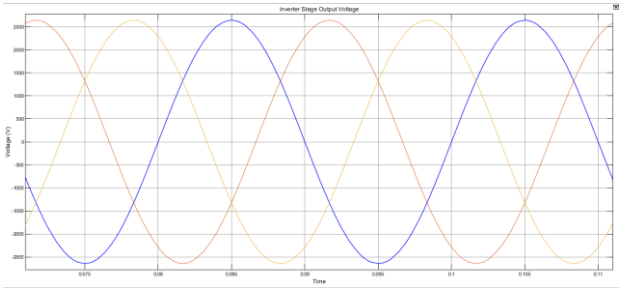

Fig. 9. The Output Three-Phase AC Waveform of the Inverter Stag

TABLE II
PARAMETERS FOR THE SIMULATION SETUP

SL. No.	*Name of the Parameters*	Value
1	Input Voltage	220V AC
2	Input Frequency	50Hz
3	Switching Frequency (S_1 and S_2)	25KHz, 40KHz
4	Duty Ratio (D_s)	0.5
5	DS Inductor (L)	0.5µH
6	DS Capacitor (C)	10µF
7	Power Rating	45KW
8	Input Filter (L_{in})	2mH
9	Input Filter (C_{in})	65µF
10	Ripple Factor (%a)	1.5625%
11	Ripple Factor(%x)	0.3185%

VII. Comparative Analysis

The proposed DS-USMC is compared with existing USMCs, such as HFTI Z-Source AC-AC, Modular Isolated UMSC, Isolated DC-link USMC, SN-USMC, and DB-USMC in terms of voltage gain, the number of switches, diodes, and passive elements. The detailed comparative analysis is exhibited in Table III. All these converters are operated at a system frequency of 50 Hz, a duty ratio of 0.5, and under similar operating conditions and load.

TABLE III
COMPARATIVE ANALYSIS OF DIFFERENT TYPES OF CONVERTERS

Converter	**Isolation**	**Voltage Gain (VG)**	**No. Switches**	**No. of Passive Elements**	**Voltage Stress**	**Remarks**
HFTI Z-Source AC–AC [18]	Yes	~2.5	12	High	High	Single-phase only, limited gain
Modular Isolated USMC [15]	Yes	~3.0	18+	Medium	Medium	Complex and bulky structure
Isolated DC-link USMC [21]	Yes	~4.0	12	High	High	High ripple, less efficient
SN-USMC (Stabilized Isolated Network) [14]	Yes	~5.0	12	Medium	Medium	Improved ripple control, moderate gain
Proposed DS-USMC	Yes	12.0	11	Low	Low	Highest gain, low switch stress

The analysis shows that the proposed DS-USMC achieves superior voltage gain compared to the others. While the number of passive elements is lower than that of the SCZ-USMC, it requires slightly more diodes and switches. However, its significantly higher voltage gain, along with the electrical isolation between input and output sections, makes it more suitable for versatile applications, including renewable energy integration, hybrid energy systems, and high-voltage applications.

VIII. Conclusion

The isolated ultra-sparse matrix converter plays a crucial role in various applications related to power and safety, where higher voltage gain and variable frequency are major concerns. This paper introduces a novel approach by proposing a USMC with an isolated duodecuple source converter and the external RCD snubber. We simulated the proposed DS-USMC using MATLAB Simulink 2020a software. The results demonstrate an excellent voltage gain of 12 and a significant reduction in voltage stress across switches. The higher voltage gain and lower switching voltage stress are achieved by integrating the duodecuple source impedance network and the external RCD snubber. However, some voltage drop was observed in the inverter stage, which may lead to a reduction in overall efficiency. If it becomes possible to maintain the same voltage from the DS stage output to the inverter stage output, this issue can be resolved. This makes a future direction.

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Conflict of Interest

The authors declare no conflict of interest in the publication process of the research article.

Author Contributions

All authors contributed to the study conception and design. Material preparation, data collection, and analysis were performed by author 1, author 3, and author 5. Author 2 supervised the entire process and was responsible for validating the results. Author 4 organized and compared the data. The first draft of the manuscript was written by author 1, and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

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