Performance Evaluation of Single Phase Transformerless Inverter for Grid-connected Photovoltaic Application

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Abstract – *This paper presents the performance evaluation of single-phase grid-connected transformerless inverter according to the level of leakage ground current. The leakage ground current ismeasured through the parasitic capacitance of PV array when the high or line transformer is omitted in the system. To prevent the electric shock, the low amplitude of leakage current is important to be achieved. The factors contribute to the leakage current, which are the PWM techniques used; parasitic capacitance and AC filter are investigated in this paper. From the Matlab Simulink simulation result, Bipolar SPWM achieves zero leakage current due to constant common mode voltage. Meanwhile the Unipolar SPWM has higher leakage current due to changing common mode voltage. However, the leakage current is reduced when the inductor filter magnitude is doubled. Generally, the efficiency of unipolar SPWM is slightly higher compared to bipolar SPWM and further improved when the inductor filter magnitude is doubled. The increase in the parasitic capacitance slightly reduces the efficiency of the inverter as well. From this finding, it is concluded that factors such as parasitic capacitance of the PV array, the PWM switching method used and the filter design must be taking into consideration in the design of the transformerless PV inverter in order to achieve minimum leakage current according to VDE-415 standard and optimum efficiency.*

Keywords: *transformerless PV inverter, leakage ground current, European Efficiency, PWM techniques, parasitic capacitance, AC filter*

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I. Introduction

Due to the low cost and high performance characteristics, the grid-connected transformerless photovoltaic (PV) inverter has become popular in the residential market for the application of solar power generation system. However, the technology of transformeless PV inverter system generates the high leakage current between PV array and the ground. The high leakage current may damage the equipment and can be hazard to human (300mA as specified in the VDE-0126-1-1 Standard) [1]. To decrease and eliminate the high leakage current, several solutions have been proposed such as switching techniques, decreasing the magnitude of parasitic capacitance and designing the suitable filter at the AC side. The leakage current is measured through the parasitic capacitors, because of the common-mode voltage would appear and lead between the PV array and ground.

The objective of this paper is to evaluate the performance of single phase transformerless grid tied PV inverter according to weighted European Efficiency method as well as observing the leakage current I_g and Common Mode Voltage V_{cmm} for the various factors such as Pulse Width Modulation (PWM) technique, parasitic capacitance and AC filter effect through MATLAB/ Simulink approach.

This paper is structured as follows. The effect of level of leakage current in the H-Bridge transformerless inverter is discussed in Section II. The equivalent circuit of common mode voltage and its derivation is presented in Section III. The simulation results of the topology proposed are discussed in Section IV. The conclusion of the simulated results is stated in Section V.

II. Effect of Level of Leakage Current

The effect of level of leakage current is presented in subsection A, B, and C. In subsection A, the switching technique chosen will bring a significant effect to the level of leakage current when using unipolar compared to bipolar PWM switching method. The parasitic capacitance also contributes to this effect and discussed in subsection B. The AC filter effect which further reduces the leakage current is presented in subsection C.

A. Fullbridge Transformerless Inverter and SPWM Strategy

Fig. **1** shows the full-bridge transformerless inverter. This transformerless inverter works with higher input voltage when compared to the inverter with transformer [2]-[3]. The performance and applicability are strongly influenced by the employed modulation scheme and the resultant voltage across the parasitic capacitors between the panel and ground [4]-[6].

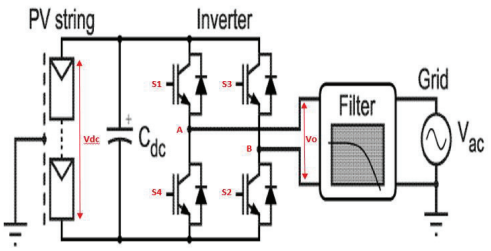


Fig. 1. Full-bridge transformerless inverter topology

The unipolar pulse width modulation (UPWM) scheme for full-bridge transformerless inverter is defined in Table I. As defined by equation (1) and shown in Fig. 2, in the UPWM scheme, the voltage, V_{cm} is equal to half of the DC link voltage, $\frac{V_{DC}}{2}$ during the active mode while during freewheeling mode, V_{cm} is equal to zero or DC link voltage, V_{DC} [7]. Therefore, the leakage current exists in the conventional full-bridge transformerless inverter depends on common-mode voltage whether during active or freewheeling mode [7]. The current ripple at twice the switching frequency and low core losses. The maximum current ripple of the unipolar scheme is four times smaller than the bipolar scheme.

TABLE I
UNIPOLAR SWITCHING SCHEME

Condition	Switch ON	Frequency switches
$V_{sine} > V_{tri}$	S_1	High
$-V_{sine} < V_{tri}$	S_2	Low
$-V_{sine} > V_{tri}$	S_3	Low
$V_{sine} < V_{tri}$	S_4	High

$$V_0 = V_a - V_b = \begin{cases} +V_{DC}, & for\ (S_1\ \&\ S_2)\ are\ ON \\ 0, & for\ (S_1\ \&\ S_3)\ or\ (S_2\ \&\ S_4)\ are\ ON \\ -V_{DC}, & for\ (S_3\ \&\ S_4)\ are\ ON \end{cases} \quad (1)$$

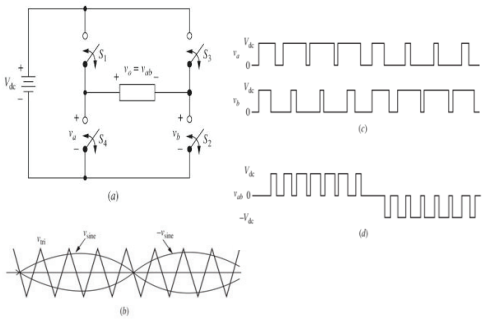


Fig. 2. Unipolar switching scheme

The bipolar pulse width modulation (BPWM) scheme of conventional full-bridge transformerless inverter is tabulated in Table II and the resulted output voltage is shown in Fig. 3 and defined by equation (2). The main advantage using BPWM is no changes in the common-mode voltage and no leakage current is generated [8]-[9]. However, bipolar switching technique has drawback which is double switching losses [8]-[9]. It is because of two diodes and two IGBT are switching at the switching frequency with whole input voltage which doubles the switching losses. Other than that, the current ripple that is produced from bipolar PWM is twice than unipolar PWM.

TABLE II
BIPOLAR SWITCHING SCHEME

Switch ON	Voltage output, V_o
S_1 and S_2	$+V_{DC}$
S_3 and S_4	$-V_{DC}$

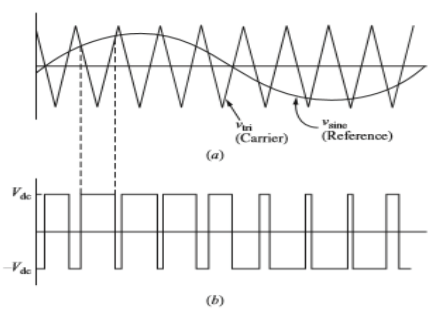


Fig. 3. Bipolar switching scheme

$$V_o = +V_{DC} \qquad for\ V_{sine} > V_{tri}$$
$$V_o = -V_{DC} \qquad for\ V_{tri} > V_{sine} \qquad (2)$$

B. Parasitic Capacitance

When transformer is not used in the PV grid connected system then ground leakage current arises through the parasitic capacitor between PV panels and ground due to existence of galvanic connection [10]. One of the important issues in the transformerless grid-connected PV system is the galvanic connection of the grid and photovoltaic system, which leads to a leakage current problem [11].

The parasitic capacitance value depends on many factors which are the PV panel and frame structure, surface of cells and distance between cells, module frame, weather conditions, humidity, dust or salt covering the PV panel and type of EMC filter [12]. Due to the large surface of the PV generator, the parasitic capacitor with respect to the ground achieves value that is higher than 200 nF/kWp in moist environments or on rainy days [13]. But other researchers say that, the parasitic capacitance is in between of 50 nF/kW to 150 nF/kW which is enough to conduct the leakage current at the switching frequency from 7 kHz to 20 kHz [4].

Other than that, several researchers state that the leakage current from solar panel has a parasitic capacitance which is in between of 10 nF/kWp to 100 nF/kWp [9]. This value produces ground currents with amplitude above the permissible level such as those linked to the standard [13]. By including damping passive components in the resonance circuit, the leakage current can be avoided or reduced. The damping elements will result in additional losses and conversion efficiency will decrease [13].

C. Effect of AC Filter

Low pass filter at the AC side for transformerless inverter is meant to reduce current harmonic injected into grid and system losses that caused from leakage current production when SPWM Unipolar is used [14]. In order to cancel the differential mode voltage from influencing the common mode voltage as derived in [1], the LCL low pass filter is chosen and the value of L_1 is same as L_2 as per derivation in [1]. Fig. 4 of [14] is the topology of the LCL low pass filter at the AC side.

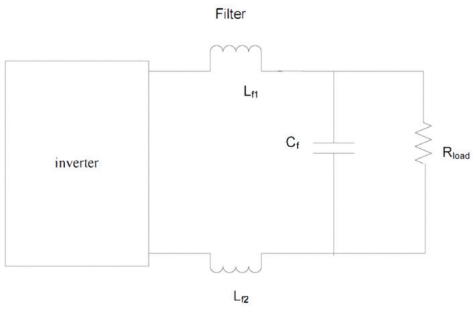


Fig. 4. LCL Low Pass AC Filter

Equation (3) defines the inductor filter parameter. The maximum ripple current is chosen between 5% to 20%. [14].

$$L_f = \frac{1}{8}\frac{V_{DC}}{\Delta_{ripple}\ f_{SW}} \qquad (3)$$

where:

Δ_{ripple} = percentage of ripple current

f_{SW} = switching frequency of the carrier signal

V_{DC} = DC voltage from PV panel

Capacitor filter parameter is defined by the reactive power absorbed in the filter capacitor as per equation (4) below, with α is the reactive power factor. The value of α is selected of less than 5% [14].

$$C_f = \frac{\alpha P_{rated}}{2\pi f_{line} V_{rated}^2} \qquad (4)$$

where:

P_{rated} = rated power output

V_{rated} = rated output voltage

f_{line} = line frequency or AC output frequency

Equation (5) defines the resonance frequency of the AC circuit. To avoid the resonance effect and ensure carrier attenuation, filter resonance frequency should be less than the carrier frequency [14].

$$f_r = \frac{1}{2\pi\sqrt{L_f C_f}} Hz \qquad (5)$$

III. Equivalent Circuit of Common Mode Voltage

Equivalent circuit for the transformerless single phase grid tied inverter from [1] is shown in Fig. 5.

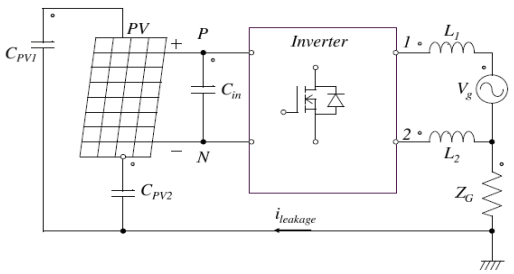


Fig. 5. Equivalent circuit of transformerless single phase grid tied inverter

Assuming the negative terminal of PV (N) is the reference point and midpoint of the bridge leg 1 and 2 as output terminal. From the definition of differentian mode, V_{CM} and V_{DM} are defined as follows.

$$V_{CM} = \frac{V_{1N} - V_{2N}}{2} \quad (6)$$

$$V_{DM} = V_{1N} - V_{2N} \quad (7)$$

Where V_{CM} is the common mode voltage, V_{DM} is the differential voltage, V_{1N} is the voltage between leg 1 and N and V_{2N} is the voltage between leg 2 and N. Taking into account equation (6) and (7), V_{1N} and V_{2N} can be expressed as:

$$V_{1N} = \frac{V_{CM} + V_{DM}}{2} \quad (8)$$

$$V_{2N} = \frac{V_{CM} - V_{DM}}{2} \quad (9)$$

Fig. 6 is the equivalent circuit of the transformerless inverter in common mode voltage mode.

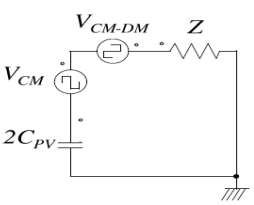


Fig. 6. Common mode voltage equivalent circuit of transformerless inverter

Where V_{CM-DM} is the influence of differential mode voltage to common mode voltage. From the cirucit shown, the commom mode voltage has influence in leakage current. There is also additional common mode voltage $V_{d\text{-}to\text{-}c}$ that can be defined as:

$$V_{d-to-c} = V_{DM} \frac{L_2 - L_1}{2(L_2 + L_1)} \quad (10)$$

Taking accont of equation (6), differential voltage with unbalanced L_1 and L_2 inductor contributes to common mode voltage which increasing the leakage current.

$$V_{TCM} = V_{CM} + V_{d-to-c} \quad (11)$$

$$V_{TCM} = \frac{V_{1N} + V_{2N}}{2} + \frac{V_{1N} + V_{2N}}{2} \frac{L_2 - L_1}{(L_2 + L_1)} \quad (12)$$

Where V_{TCM} is total high frequency common mode voltage. By considering only one of the inductor (L_1 or L_2), equation (12) is reduced for example by considering L_1 only:

$$V_{TCM} = \frac{V_{1N} + V_{2N}}{2} - \frac{V_{1N} - V_{2N}}{2} = V_{2N} \quad (13)$$

Therefore, it is concluded that if $L_1 = L_2$, then the common mode voltage can be expressed as,

$$V_{TCM} = \frac{V_{1N} + V_{2N}}{2} = V_{CM} \quad (14)$$

From the model presented in Fig. 6, two ways to eliminate or reduce leakage current in PV system are as follows:

(a) To design sinusoidal pulse width modulation (SPWM) strategy so the V_{CM} is kept at constant for symmetrical filter topologies with zero $V_{CM\text{-}MD}$.
(b) To match circuit parameter in the way that the sum of $V_{CM\text{-}MD}$ and V_{CM} is constant.

IV. Simulation Results

The simulation circuit of the single phase transformerless inverter is shown in Fig. 7 using MATLAB Simulink. The circuit is modified from the existing preinstalled simulation circuit of single phase grid connected inverter inside the Simulink.

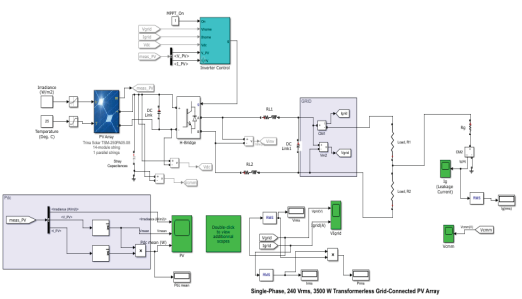


Fig. 7. Simulation circuit of Single Phase Transformerless Grid-Connected PV Inverter (please refer Appendix for the details)

The parameter to be fixed are as per Table III(A).

TABLE III(A)
FIXED SIMULATION PARAMETERS

No.	Parameters	Values
1.	Rated DC Voltage	400V
2.	Rated AC Voltage	240V_{rms}
3.	Rated AC Frequency	60Hz
4.	Inverter Rated Power	3,500VA
5.	PV Array	Trina Sonar TSM-250PA05.08 14 module string 1 parallel strings Power per Module: 249.8 W Total Power: 3,497.2W
6.	Irradiance	250 W/m^2 (from 0 - 0.4 s) 750 W/m^2 (from 0.4 to 1.2 s)
7.	Temperature Module	25°C
8.	Filter Arrangement	LCL
9.	Capacitor Filter (C_f)	3µC
10.	Parasitic Inductor and Capacitor Filter Resistor	0.005Ω
11.	MPPT Mode	On

The parameter to be varied are as per Table III(B**)** below.

TABLE III(B)
VARIABLE SIMULATION PARAMETER

No.	Parameters	Values
1.	Pulse Width Modulation (PWM)	Bipolar SPWM at 1890Hz Unipolar SPWM at 3780Hz
2.	Paracitic Capacitance (C_p)	4nF (Initial) 16nF
3.	Inductor Filter (L_f)	L_f: 4mH (Initial) 2xL_f: 8mH
4.	Load	100%: 50Ω 50%: 25Ω 30%: 15Ω 20%: 10Ω 10%: 5Ω 5%: 2.5Ω

The formula of European Efficiency is shown in the equation (15). This European Efficiency formula is reflected in the efficiency performance. The weighting factor of European efficiency is used to measure the performance and show the optimal value that can be obtained for European efficiency. This formula is proposed by Joint Research Centre and has served as a guideline for almost every inverter datasheet [15].

$$\eta_{EU} = 0.03(\eta_{5\%}) + 0.06(\eta_{10\%}) + 0.13(\eta_{20\%}) + 0.10(\eta_{30\%}) + 0.48(\eta_{50\%}) + 0.20(\eta_{100\%}) \quad (15)$$

The European efficiency is the efficiency which is validated by a variation of load such as full-load efficiency ($\eta_{100\%}$), half-load efficiency ($\eta_{50\%}$), 30% of full-load efficiency ($\eta_{30\%}$), 20% of full-load efficiency ($\eta_{20\%}$), 10% of full-load efficiency ($\eta_{10\%}$), and 5% of full-load efficiency ($\eta_{5\%}$).

The value of C_p tested as per suggested in [16] and [9]. For the purpose of this experiment, the tested value of parasitic capacitance are 4nF and 16nF. The configuration of the LCL filter and its default parameter L_f and C_f is as suggested in [14].

The calculation of common mode voltage changes ΔV_{cmm} and efficiency η is define in the following equations (16) and (17).

$$\Delta V_{cmm} = V_{cmm(\max)} - V_{cmm(\min)} \quad (16)$$

$$\eta = \frac{P_{AC(rms)}}{P_{DC(mean)}} \; x\,100 \quad (17)$$

where:

$V_{cmm(\max)}$ = maximum common mode voltage

$V_{cmm(\min)}$ = minimum common mode voltage

$P_{ac(\mathrm{rms})}$ = AC RMS power output

$P_{dc(\mathrm{mean})}$ = DC mean power input

The results from the simulation are tabulated in Table IV.

TABLE IV
SIMULATION RESULTS

No.	Variable Parameter	Load (%), 100% at 50 Ω	I_g (mA)	ΔV_{cmm}	η (%)
1.	Bipolar 3760Hz, C_p 4nF, L_f	100	0.006	4.70	92.53%
		50	0.003	2.18	99.52%
		30	0.003	1.22	100.00%
		20	0.004	1.42	100.00%
		10	0.013	3.92	100.00%
		5	0.045	28.48	82.67%
		Average I_g / ΔV_{cmm} and η_{EU}	**0.012**	**6.99**	**97.75%**
2.	Unipolar 1890Hz, C_p 16nF, L_f	100	346.00	1135.00	95.22%
		50	183.30	887.90	99.92%
		30	69.13	411.10	100.00%
		20	88.89	388.10	97.50%
		10	72.26	285.70	99.67%
		5	635.30	1400.50	80.60%
		Average I_g / ΔV_{cmm} and η_{EU}	**232.48**	**751.38**	**98.08%**
3.	Unipolar 1890Hz, C_p 4nF, L_f	100	159.10	1242.00	95.38%
		50	86.87	714.60	100.00%
		30	30.40	352.40	98.29%
		20	12.82	323.00	99.11%
		10	48.69	330.20	99.68%
		5	247.90	1074.60	78.79%
		Average I_g / ΔV_{cmm} and η_{EU}	**97.63**	**672.80**	**98.13%**
4	Unipolar 1890Hz, C_p 4nF, 2 x L_f	100	113.60	1190.40	99.31%
		50	58.10	589.30	100.00%
		30	31.42	439.80	100.00%
		20	101.00	800.20	98.44%
		10	0.00	461.10	99.76%
		5	0.00	491.10	100.00%
		Average I_g / ΔV_{cmm} and η_{EU}	**50.7**	**661.98**	**99.65%**

Based from the above Table IV, the comparison graph of average leakage current I_g and common mode voltage changes ΔV_{cmm} for each variable parameter are projected and shown in Fig. 8 below.

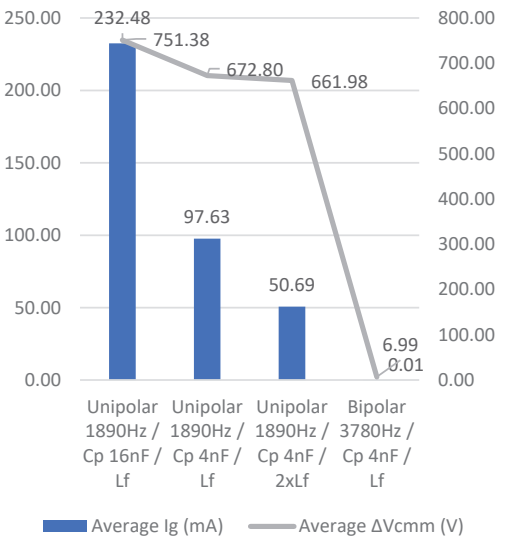
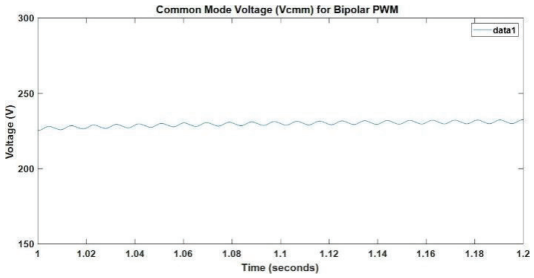


Fig. 8. Comparison of average I_g and ΔV_{cmm}

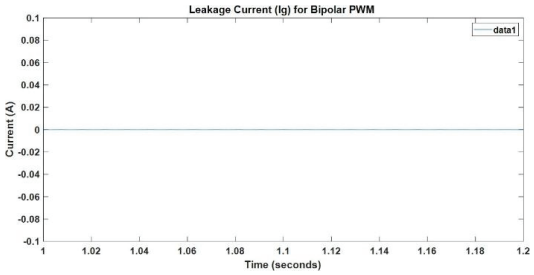
From Fig. 8, it is clearly shown that I_g is high when the ΔV_{cmm} is large, with the highest I_g and ΔV_{cmm} are from Unipolar PWM with C_p of 16nF, and I_g significantly decreasing in half and ΔV_{cmm} decreasing in 10% when the C_p is reduced to the quarter. Then, the I_g is decreased almost in half when the L_f value is doubled and the corresponding ΔV_{cmm} is slightly decreased to 2%.

When the PWM is switched to bipolar with double of unipolar frequency, the ΔV_{cmm} is very small and the I_g is almost non-existent. This confirms with the analysis done by [15] that states when common mode voltage, V_{cmm} is constant due to the modification of modulation strategy, the leakage current, I_g is reduced or eliminated and further validated by the V_{cmm} and I_g waveform from simulation for both bipolar and unipolar as shown in Fig. 9(a) to (b) and

Fig. 10(a) to (b). The rms value of the V_{cmm} for bipolar PWM 3780Hz is 230.4V, while I_g value is almost zero.

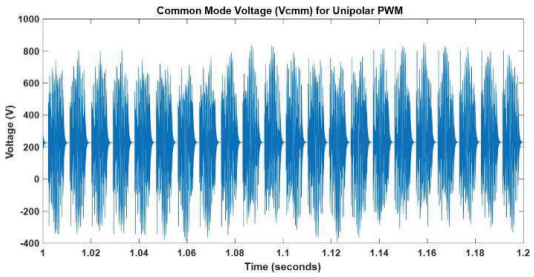


(a)

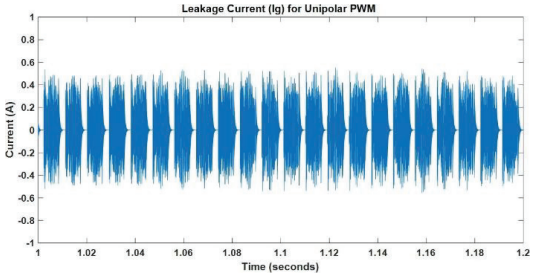


(b)

Fig. 9 (a) V_{cmm} for bipolar PWM 3780Hz, which shows the common mode voltage is almost constant with $V_{cmm\ rms}$ is 230.4 V and (b) I_g for bipolar PWM 3780Hz, which shows the leakage current is zero when common mode voltage is almost zero.



(a)



(b)

Fig. 10 (a) V_{cmm} for unipolar PWM 1890Hz, which shows the changes of common mode voltage is large and continuous and (b) I_g for unipolar PWM 1890Hz, which shows the leakage current is increasing when the common mode voltage is not constant and voltage changes is increasing

The high leakage current on unipolar PWM is contributed by the superimposed high frequency signal effect on common mode voltage compared to bipolar PWM which has sinusoidal waveform with the amplitude of $V_{ac}/2$ at line frequency as stated in [8].

Also from Table IV, the comparison graph of average leakage current I_g and weighted European efficiency η_{EU} for each variable parameter are projected and shown in Fig. 11.

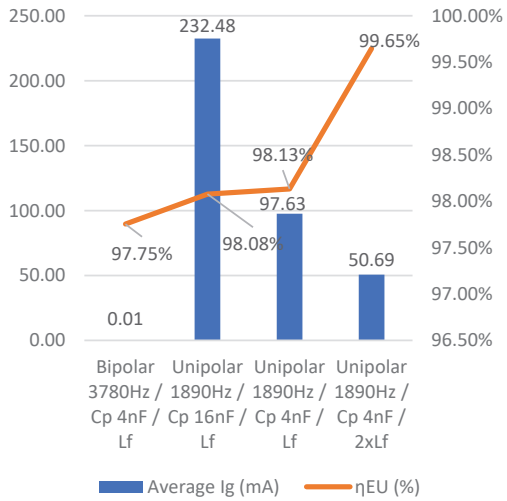


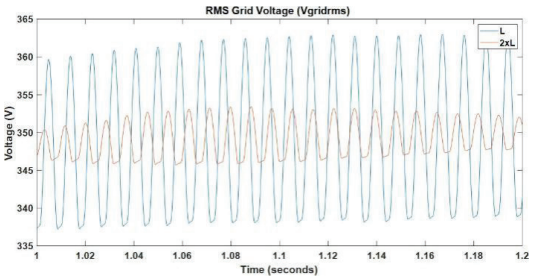
Fig. 11. Comparison of average I_g and η_{EU}

From the above Fig. 11, the efficiency for unipolar PWM is slightly increased about half percent compared to bipolar PWM despite producing almost non-existent of leakage current. In order for bipolar PWM to match similar efficiency performance of unipolar PWM, its frequency need at least to be doubled of unipolar PWM. Thus, it brings the advantage of filter design and selection of power electronic component for unipolar PWM transformerless inverter as it requires small sizing of the inductor and capacitor filter and low cost switching transistor as it operates much more less of the switching frequency compared to bipolar PWM.

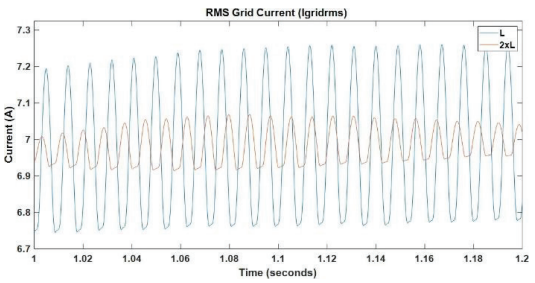
For the effect of parasitic capacitance C_p on unipolar PWM, there is slight increase in the efficiency about less than half percent when the C_p magnitude is reduced to quarter despite significant reduction of leakage current about half. This shows that the increase in efficiency is insignificant on unipolar PWM with decreasing C_p value. But the significance of parasitic capacitance factor to the leakage current need to be considered seriously in designing unipolar PWM transformerless inverter. The contribution of parasitic capacitances comes from PV array and its magnitude depends on weather conditions

and physical structure of the array. It can be estimated according to the physical dimensions of the PV array and its grounded frame area as stated in [8].

For the effect of the inductor filter L_f on unipolar PWM, there are significant increase of more than 1% efficiency when the inductor value is doubled from L_f (4mH) to 2 x L_f (8mH) and the leakage current is also significantly reduced in half. The significant increase of efficiency is not only caused by the reduction of leakage current due to the changes of the filter impedance, but also comes from the contribution of grid voltage and current ripple reduction thus reducing THD of the power delivered to the load as validated by the $V_{grid,rms}$ and $I_{grid,rms}$ waveform from simulation as shown in Fig. 12(a) and (b) below.



(a)



(b)

Fig. 12 (a). Reduction of RMS Grid Voltage ripple when the inductor value is doubled and (b) reduction of RMS Grid Current ripple when the inductor value is doubled

The $V_{grid,rms}$ and $I_{grid,rms}$ are 348.7 V and 6.975 A respectively for initial inductor value while the $V_{grid,rms}$ and $I_{grid,rms}$ are 349.1 V and 6.983 A respectively if the inductor value is doubled from the initial.

V. Conclusion

This simulation presents the comparison and analysis of various recently proposed single-phase transformerless PV inverter topology. It is shown that three strategies have been commonly used for reducing leakage current and also increasing efficiency of the transformerless PV inverter.

Factors such as parasitic capacitance of the PV array, the PWM switching methods used and the filter design must be taking into consideration to design the transformerless PV inverter in order to achieve minimum leakage current according to VDE-415 standard and optimum efficiency.

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Appendix

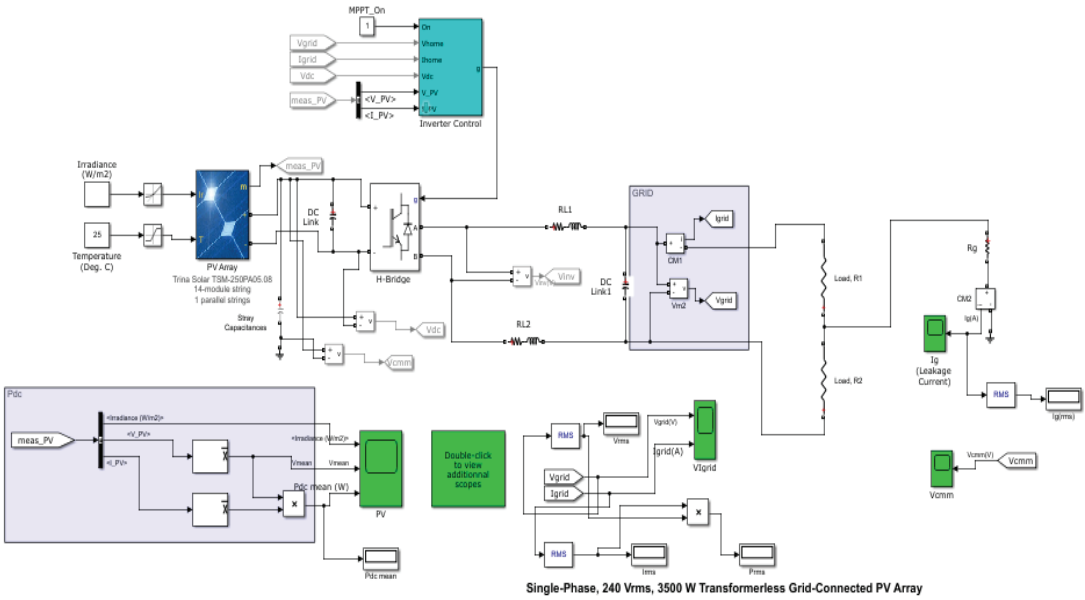

Fig. A1. Simulation circuit of Single Phase Transformerless Grid-Connected PV Inverter