Capacitor Voltage Balancing with Reduction of Arm Current and THD Control of MMC: A Modified Triangular Injection Approach

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Abstract – *For high power applications, in recent time, Modular Multilevel Converter (MMC) has become popular because it consists of number of DC sources. Stair voltage output waveform of this type of converter can be controlled by different modulation techniques. Harmonic profile of a converter with a modulation scheme much depends on the carrier frequency used in it. On the other hand, with the importance of lower Total Harmonic Distortion (THD), the arm current control is also the necessity to drive an MMC in smooth operation. Moreover, imbalance of the Sub-Module (SM) capacitor voltages affects the arm current as well as the life time of the capacitors. In this way the overall performance of the converter could be affected. As a result, several efforts of research in this area focused on to minimize the THD, balance the capacitor voltage of Sub-module (SM) and to control the arm current of the converter. This paper proposed a modified triangular injection modulation structure for MMC converters to maintain minimum harmonic profile as well as to achieve lower arm current and capacitor voltage balancing of SM within a single algorithm structure. Several well-known modulation methods have been compared with the proposed method so that percentage of THD and the arm current can be identified as minimum and SM's capacitor voltages could be compared.*

Keywords: *MMC, THD, arm current, SM voltage*

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I. Introduction

Voltage Source Inverter (VSI) topologies have been accepted for its high operating voltage as well as lower losses, in many power converter applications. Modular Multilevel Converter (MMC) is one type of VSI where several modulation techniques have been discussed in literature. Depending on the switching frequency in a modulation, a method could be high frequency modulation or low frequency modulation technique. Selective Harmonic Elimination PWM (SHE-PWM) is a low frequency switching method, which depends on look up tables [1]. However, among different high frequency PWM methods phase-shifted or carrier deposition are the most common for easy control of operation. The sinusoidal pulse width modulation (SPWM), Bus Clamping PWM (BCPWM), Third Harmonic injected Pulse Width Modulation (THPWM) techniques are also working well in multilevel converters [2]-[3]. The Circular Space Vector Modulation (CSVM) is considered as a standard for pulse width modulation techniques [4]. However, the main drawback of CSVM based modulation is the redundancy of the output, which in turn increases the complexity [5]. There are also some level-shifted or sub-harmonic deposition modulation which shows good THD profile at higher number of output level such as the Phase Deposition (PD) [6]. A modified PD method called triangular injection has been applied to both MMC and cascaded bridge converter to achieve lower THD profile by M.A. Munjer et. al [6]. The work found a lower THD profile, but the arm current investigation was absent. In this paper an algorithm has been proposed for MMC, which is based on triangular injection method. This single algorithm structure has confirmed minimum harmonic profile as well as lower arm current and a balanced capacitor voltage of the Sub-module (SM). Several well-known modulation methods have been compared with the proposed method.

II. Structure of MMC

The three-phase configuration of Modular Multilevel Converter (MMC) has been shown in Fig. 1 where each SM is composed of only two switches in cascade and a capacitor paralleled to the switches. Depending on the

switching states of an SM for MMC, an arm of any leg can be considered as a voltage source that can be regulated. The number of SM inserted to the current path can be considered as the number of sources having voltage V_c. If insertion index *n(t)* which sets the number of sub-modules inserted to the current path, N sub-modules in an arm containing each a capacitance C makes total capacitance C_{arm}, then the applicable capacitance to the inserted SM becomes $C_{arm} = n(t) * C_m$. The upper and lower arm currents can be expressed as,

$$I_p = \frac{C_{arm}}{n_p} \times \frac{d\sum(V_{cp})}{dt} = I_{circ} + \frac{I_l}{2} \quad (1)$$

$$I_n = \frac{C_{arm}}{n_n} \times \frac{d\sum(V_{cn})}{dt} = I_{circ} - \frac{I_l}{2} \quad (2)$$

$$\frac{dI_{circ}}{dt} = \frac{V_{dc}}{2L_{arm}} - \frac{R_{arm}}{L_{arm}} \times I_{circ} - ¥(V_C) \quad (3)$$

$$¥(V_C) = \frac{n_p}{2L_{arm}}(\sum V_{cp}) + \frac{n_n}{2L_{arm}}(\sum V_{cn}) \quad (4)$$

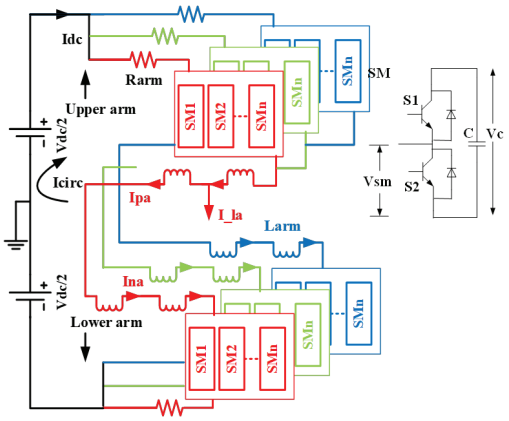

Fig. 1. Circuit diagram of three phase MMC.

where I_{circ} is loop current that circulates between each phase leg and the dc-link, n_p and n_n are upper and lower arm insertion index respectively. Under balanced load conditions, the dc-link current I_{dc} is shared equally between the three phase legs. V_{cp} and V_{cn} are individual SM capacitor voltages of positive and negative arm. Equation (3) can be calculated from (1) and (2). Finally, a continuous model of a phase leg of MMC is obtained as in (5) by using (1), (2) and (3) which best describes the operation principal of MMC.

$$\frac{d}{dt}\begin{bmatrix} I_{circ} \\ \sum V_{cp} \\ \sum V_{cn} \end{bmatrix} = \begin{bmatrix} -\frac{R_{arm}}{L_{arm}} & -\frac{n_p}{2L_{arm}} & -\frac{n_n}{2L_{arm}} \\ \frac{n_p}{C_{arm}} & 0 & 0 \\ \frac{n_n}{C_{arm}} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{circ} \\ \sum V_{cp} \\ \sum V_{cn} \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{2L_{arm}} \\ \frac{n_p}{2C_{arm}} I_l \\ \frac{n_n}{2C_{arm}} I_l \end{bmatrix} \quad (5)$$

III. Methodology

A. Modulation Method

Nowadays, to achieve minimum THD several modulation techniques are available in literature such as CSVPWM, SPWM, THPWM, SDBCPWM, TDBCPWM, and TRPWM [7]-[9]. The following techniques differ from each other by their reference signals. Figure 3 shows the reference signals of the SPWM, CSVPWM, SDBCPWM, and THPWM modulation approach.

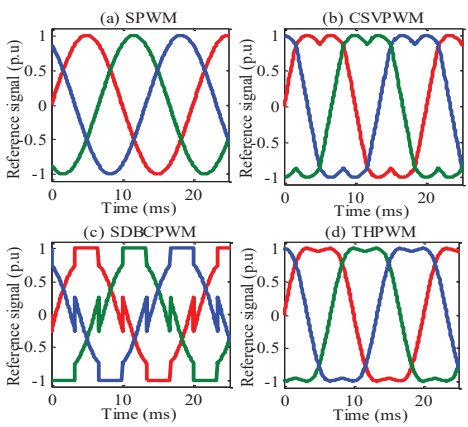

Fig.2. Reference signals for different modulation schemes.

The reference signals of the triangular injection modulation scheme can be represented as in Fig. 3(a). In this method, a triangle signal represented by δ(ξωt) is added with the sine wave containing the desired frequency of the converter output but the reference and carriers should be same when they will be added up. For having (n+1) level of output voltage there should have n number of carriers shown in Fig. 3(b). The frequency of the triangular signal for the current scheme maintains a multiple factor ξ concerning the frequency of the reference signal, which can be noticed from equations (6) to (8). The relative comparison between the reference and carriers

generates pulses which denotes the insertion index n^{abc} for the switching devices of the converter as represented in (9) [6],[10].

$$M_a = A_m \sin \omega t + a_m \delta(\xi \omega t) \quad (6)$$

$$M_b = A_m \sin (\omega t - 120°) + a_m \delta(\xi \omega t) \quad (7)$$

$$M_c = A_m \sin (\omega t + 120°) + a_m \delta(\xi \omega t) \quad (8)$$

$$n^{abc} = \mathcal{R}\{M_{abc}, \ell_k \delta(\xi \omega t)\}_{k=1,..n} \quad (9)$$

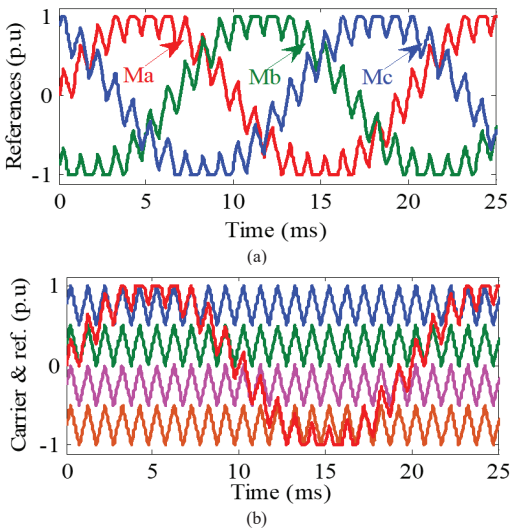

Fig. 3. (a) Reference signals (b) carrier with reference signal of the proposed modulation scheme.

B. Voltage balancing methods

In literature, there are number of methods to maintain equal amount of voltage for the SM capacitor. In this work two methods known as Sort & Selection method (S&S) and carrier rotation method are analyzed to be incorporated with the triangular injection modulation approach.

According to S&S method, capacitor voltages of all the sub-modules and polarity of the arm current are measured. All the capacitor voltages in an arm are measured and sorted from the highest to the lowest. The number of "required" SM (N_c) to be connected with the upper and lower arm's current path should be determined. Fig. 4 shows the procedure to determine N_c. At the time of comparing reference and carrier, if the reference is greater than a carrier, one SM for this carrier should be inserted to the current path, corresponding to increment of N_c by one. On the other hand, if the reference is lower, one SM should be bypassed, without changing the value of N_c. All the N carriers are compared with the reference and N_c is determined [10].

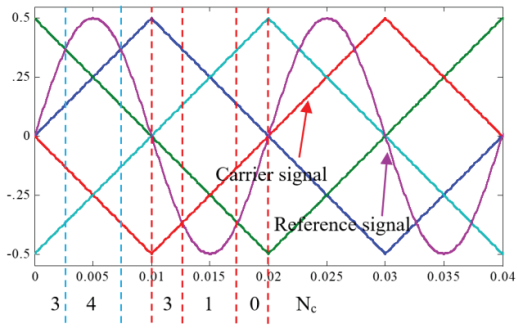

Fig. 4. Determination of Nc in Sort & Selection (S&S) Method.

Moreover, a method called carrier rotation is used for the capacitor voltage balancing where sub-module capacitor voltage measurement and arm current polarity are not required [11]. This method is governed with the common reference signal and individually assigned carrier signal for each SM. In order to equate insert/bypass times of different submodules, the participation of carriers should be changed periodically. By this way, insert/bypass durations of sub-modules are equated to each of them. Therefore, a balance submodule capacitors voltage could be achieved. In Fig. 5 rotated carriers for N=4 is illustrated. As seen from figure, each carrier has been shifted to higher magnitude for 20ms. When a particular carrier has reached to a maximum value (0.5) of the carrier band, it is shifted to minimum value (-0.5) of the band.

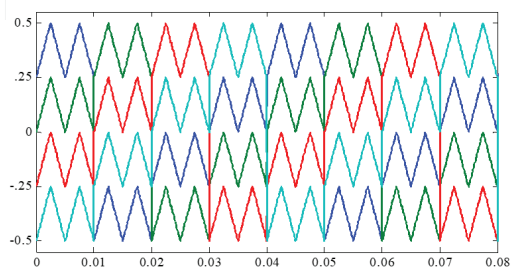

Fig. 5. Carrier Rotation for Voltage Balancing.

C. Proposed Balancing Algorithm

For the conventional Sine PWM (SPWM) method, the number of carriers required to be compared with the reference signal is equal to the number of SM used in either positive or negative arm of a phase of the converter. As a result, the pulses for the switching devices are generated in such a way that conduction period of SM decreases with the distance of the neutral point to SM connected in an arm of a phase of the converter. In this way an unbalanced charging voltages will be carried out by the capacitor connected with the SM. The most upper capacitor in an arm is being charged in lower voltage where the capacitor at nearest to the neutral get charged at higher voltage level.

This causes a circulating current which causes a variation in the life time of the SMs.

In this work an improved level-shifted carrier rotation pulse-width modulation scheme has been proposed to balance the voltage of the floating capacitor. This method also maintains a lower THD by avoiding some major disadvantages found in the conventional voltage balancing methods, such as the use of extra switching action, interference with output voltage and periodic carrier rotation which lead to high performance of the converter. To do so, the triangular injection method has been incorporated.

In the present work, the level of the carriers is maintained according to the magnitude of the capacitor voltage of the corresponding SM. Fig. 6 shows the flow chart of the proposed capacitor voltage balancing algorithm. At the very beginning, the algorithm verifies that all SMs capacitors voltages are same or not. If all the voltages are same, the corresponding carrier signal will be arranged in the same level. The magnitude of voltage will determine at which level the carrier will be arranged. On the other hand, if the values of voltage are not equal then they are sorted in large to small order. The ranking of largest voltage would be first, next highest voltage's rank will second and sequentially third up to k. Now the corresponding carriers of voltages that ranked from 1 to $k/2$ will be arranged at the lower half (0 to -11) of the carrier rotation window as shown in Fig. 7 and rest carriers would be arranged at the upper half (0 to 1) of the window.

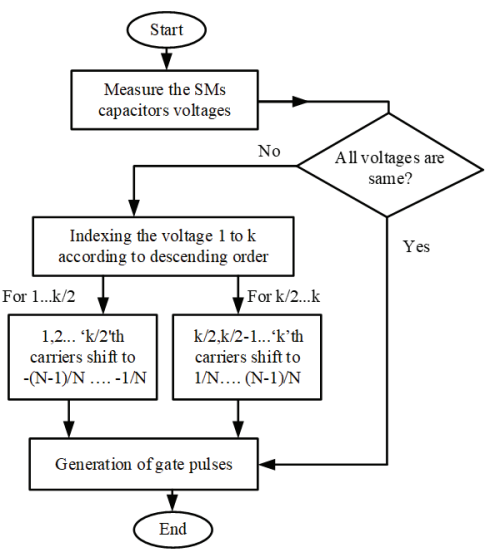

Fig. 6. Flow chart of the proposed balancing algorithm.

According to the proposed algorithm a voltage balancing module for an arm of MMC in MATLAB Simulink environment is shown in Fig. 8. The input terminals of this module, v_{c1}, v_{c2}, v_{c3}, v_{c4} corresponds to the capacitor voltage input terminal of a specific arm.

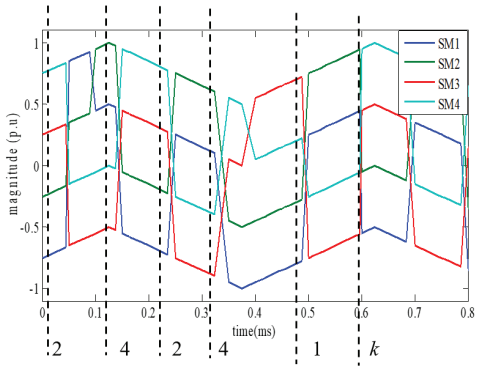

Fig. 7. Carrier rotation according to the rank of SMs capacitor voltage.

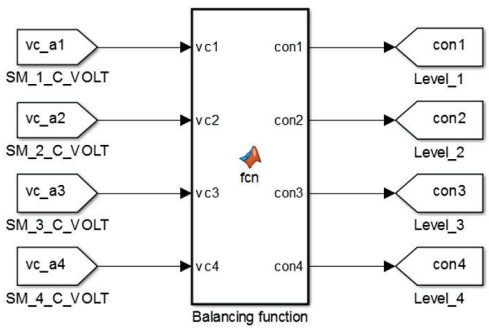

Fig. 8. Capacitor voltage balancing module in MATLAB Simulink

For both positive and negative arm of the converter, two of the modules will be needed. Taking the voltages, it sorts the values of the voltage according to descending order and rank them from 1 to N as N number of carriers is required for number of N SM.

The ranked-1 (one) SM's capacitor voltage implies that corresponding carrier stands on the lower level of the carrier rotation pane. Similarly, the higher ranked SM's capacitor voltage implies that corresponding carrier stands on the lower level of the carrier rotation pane. However, the other ranked voltage's corresponding carrier rotates to higher or lower level of the carrier pane depending on the voltage. The above Fig. 8 shows the carrier rotation pane of upper arms for 5-level MMC.

It can be seen that, as corresponding capacitor voltages of SM1 and SM4 are higher and lower ranked accordingly, they interchanged their level but carriers which relative to SM2 and SM3 stepped down and up instantly. For an example, as in case of SM3's capacitor voltage, at first instant its voltage rank was k=2. In order to have a uniform charging of the capacitors, corresponding carrier should be stepped down on the carrier pane. Capacitor voltage was lower compared to any other capacitor voltage at specific arm. For that, carrier signal of SM3 was placed to rank=4. After that its voltage starts to rise and at instant its voltage goes to more than SM4 but less than the other. As a result, corresponding carrier get a rank=2.

IV. Simulation and Results

Circuit configuration of the simulated system in MATLAB Simulink is shown in Table I. The dc-link is set to be 800 V and the ac side line-to-line voltage of the system is set at 325 V_{rms} 50Hz. Rated power of the converter is 5 kVA with 6.25 A_{rms} output current. Base impedance of the system is calculated in equation (10).

$$Z_{base} = \frac{V_{base}^2}{S_{base}} = \frac{(325)^2}{5000} = 21.125\Omega \quad (10)$$

TABLE I
SIMULATED CIRCUIT PARAMETERS (WITHOUT LOAD)

Meaning	Value
Dc-link voltage	800V
Fundamental frequency	50Hz
Carrier frequency	2.5kHz
Number of submodules per arm	4
Arm inductance	50mH
Arm resistance	400Ω
Sub module capacitance	500μF
Modulation index	1

The sub-module capacitors selection is based on maximum total energy stored in the converter and converter rated power. Energy-power ratio (EP), which is used in (11) should be kept in a range of 10 J/kVA to 50 J/kVA, depending on the application and converter [11]. In order to keep the EP equals to 48 J/kVA, the value of capacitor would be as,

$$C = \frac{EP \times N \times S_n}{3V_{dc}^2} \quad (11)$$
$$= \frac{48 \times 10^{-3} \times 4 \times 5 \times 10^3}{3 \times (800)^2} = 5 \times 10^{-4}$$
$$= 500\mu f$$

In order to satisfy the following equation (12), the fundamental frequency of the converter should be above the highest resonant frequency, which results in big values of L_{arm} and/or C values. Therefore, neither the fundamental frequency nor the harmonics coincide with the resonant frequency [12].

$$L_{arm}C > \frac{5N}{24\omega_0^2} \quad (12)$$
$$\Rightarrow L_{arm} > \frac{5 * 4}{24 * (2\pi * 50)^2 * 500 * 10^{-6}}$$
$$\Rightarrow L_{arm} > 16.68 \times 10^{-3}$$
$$\Rightarrow L_{arm} > 16.68\, mH$$

Based on the above, the arm inductor value is fixed to 50 mH in the simulation work.

The output phase voltage signal (without load) of the converter and the corresponding THD profile is shown in Fig. 9(a) and 9(b) respectively. On the other hand, Fig. 9(c) and 9(d) depicts the line to line voltage of the converter and the corresponding THD percentage. It can be seen that the THD of phase voltage and line voltage are 20.55% and 17.67% respectively.

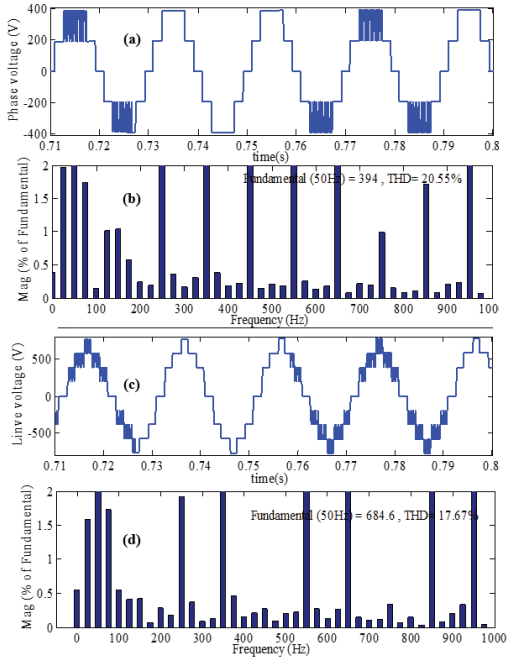

Fig. 9. Output waveform of (a) phase voltage (b) THD of phase voltage (c) line voltage (d) THD of line voltage.

The voltage levels of sub-module capacitors using different methods of modulation at any arm is presented in Fig. 10. Capacitor voltages of sub-modules using SPWM, THPWM, SDBCPWM, SVPWM and the proposed method has been arranged in Fig. 10 (a), (b), (c), (d) and (e) respectively. It is obvious that the fourth sub-module (SM4) capacitor voltage is greater than any others for any modulation methods. The reason is that, the highest voltage should be found at capacitor of the SM which connected at the nearest to the neutral point of the converter. the fourth sub-module (SM4) was connected at adjacent to the neutral point and SM1 was at far distance. All capacitors were charged at equal voltage when using the proposed method of modulation which can be seen from Fig. 10(e).

The arm current waveforms of the simulated converter based on SPWM, THPWM, SDBCPWM, SVPWM and proposed methods are shown in Fig. 11(a), (b), (c), (d) and (e) respectively. The proposed modulation has confirmed a lower arm current in comparison with other methods which can be observed from Fig. 11(e).

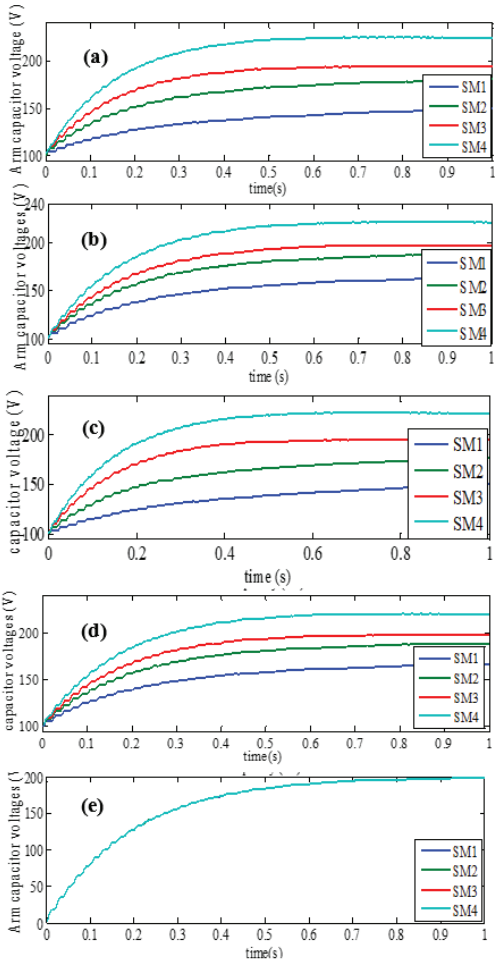

Fig. 10. Output waveform of capacitor voltages of sub-modules using (a) SPWM (b) THPWM (c) SDBCPWM (d) SVPWM (e) proposed method.

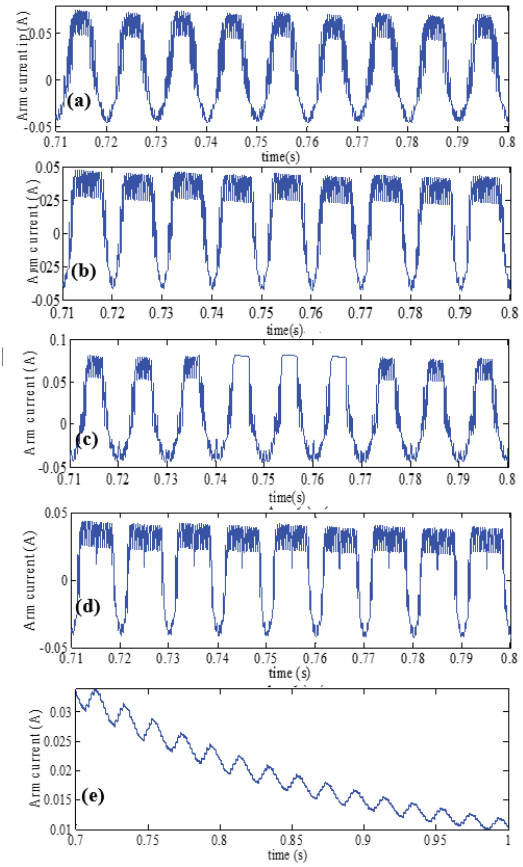

Fig. 11. Output waveforms of arm current using (a) SPWM (b) THPWM (c) SDBCPWM (d) SVPWM (e) proposed method.

V. Summary and Conclusion

Triangular injection modulation strategy has been used in this work in modified form to reduce the THD as well as arm current and to balance the capacitor voltage of the SM. All simulation results revealed some important outcomes about the modulation methods that have been applied on a typical MMC device. Table II shows the summary of the simulation which was performed in this work. In comparison with the phase voltage THD, th proposed method shows a 20.55% THD which is lower than in case of any other switching methods that have been performed in the analysis. Having a close look on the THD level of line voltage of the MMC with abovementioned configuration, a lower value of THD was achieved in case of SVPWM. However, the corresponding phase voltage THD was quite high which is 31.60%, higher than the lowest profile. In this regard, the proposed algorithm will perform with lower THD profile in both of phase and line voltage for the MMC device. Moreover, in search of capacitor voltages by different method (without proposed method) from Table II, it can be seen that the magnitude of voltages for different SM are not same and it fluctuates in range between 119 to 224. In case of the proposed modulation, the SM capacitor voltages were all in a same level between 193 V to 194 V.

The proposed method has also confirmed a lower arm current at 32 mA in comparison with the others. Considering the THD profile, capacitor voltage and arm current, the proposed method has shown a good data point. It can be noticed that although the proposed technique performs well in respect to the THD profile, arm current and SM capacitor voltage balancing, the performance analysis of the proposed method in the view of switching and conduction losses of the switching devices should be analyzed in the future work

TABLE II
SUMMARY OF RESULTS

Methods		SPWM	THPWM	SDBCPWM	SVPWM	Proposed
Phase voltage THD (%)		29.36	29.87	33.33	31.60	20.55
Line-to-line voltage THD (%)		17.53	15.62	19.83	15.59	17.67
SM capacitor voltage (Vc)	SM1	145	160	143	162	193
	SM2	176	185	172	185	193
	SM3	193	195	195	197	194
	SM4	224	222	222	119	194
Arm current (i_p) (mA max) (without load)		70	50	80	45	32

References

[1] BARIŞ ÇİFTÇİ, "Selection of suitable PWM switching and control methods for modular multilevel converter drives" M. Sc thesis, Middle East Technical University, December 2014.

[2] Li, B., Yang, R., Xu, D., Wang, G., & Wang, W. "Analysis of the Phase-Shifted Carrier Modulation for Modular Multilevel Converters", IEEE transaction of Power Electronics, Jan 2014.

[3] N. V. Nguyen, B. X. Nguyen, and H. H. Lee, "An optimized discontinuous PWM method to minimize switching loss for multilevel inverters," *IEEE Trans. Ind. Electron.,* vol. 58, no. 9, pp. 3958–3966, Sep. 2011.

[4] T. D. Nguyen, J. Hobraiche, N. Patin, G. Friedrich, and J. Vilain, "A direct digital technique implementation of general discontinuous pulse width modulation strategy," *IEEE Trans. Ind. Electron.,* vol. 58, no. 9, pp. 4445–4454, Sep. 2011.

[5] Ghazal Falahi, Wensong Yu, Alex. Q. Huang, "THD Minimization of Modular Multilevel Converter With Unequal DC Values" IEEE Energy Conversion Congress and Exposition (ECCE) September 2014): pp. 2153-5158.

[6] M. A. Munjer, M. R. I. Sheikh, M. A. Alim, V. Boddapati, and M. A. Musaib, "Minimization of THD for Multilevel Converters with triangular injection approach," 2018 3rd International Conference for Convergence in Technology (I2CT), Pune, 2018, pp. 1-4.

[7] S. Allebrod.; R. Hamerski.; R. Marquardt., "New transformerless, scalable Modular Multilevel Converters for HVDC-transmission," Power Electronics Specialists Conference, June 2008.

[8] Saeedifard, Maryam, and Reza Iravani. "Dynamic performance of a modular multilevel back-to-back HVDC system." *Power Delivery, IEEE Transactions on* 25.4 (2010): 2903-2912.

[9] M. R. Islam, Y. G. Guo, and J. G. Zhu, "A high-frequency link multilevel cascaded medium-voltage converter for direct grid integration of renewable energy systems," *IEEE Trans. Power Electron*., vol. 29, no. 8, pp. 4167–4182, Aug. 2014.

[10] M. A. Munjer, M. R. I. Sheikh, M. A. Alim, V. Boddapati and M. A. Musaib, " Minimization of THD for MMC with triangular injection approach" *International Conference on Electrical, Electronics, Computers, Communication, Mechanical and Computing (EECCMC-2018)*, Tamil Nadu, India, 2018.

[11] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pp.1-10, 2-6 Sept. 2013.

[12] S. Sedghi, A. Dastfan, and A. Ahmadyfard, "A new multilevel carrier based pulse width modulation method for modular multilevel inverter," *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on*, pp.1432-1439, May 30 - June 3 2011.